Insulating Biomaterials
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Introduction

Micromachining and integrated circuit technologies for neuroprostheses are producing functional devices for interfacing with relatively large numbers of neurons in small volumes of neural tissue while causing minimal damage to the neural structure. Protection of these devices requires development of an improved understanding of potting materials suitable for silicon devices and development of suitable materials that can be deposited as conformal thin films. Some of the possible long term failure modes for implantable electronic devices include:

- Lead wire insulation failure.
- Encapsulation failure.
- Failure at the interfaces between materials.
- Substrate corrosion.
- Surface dielectric corrosion.
- MOS gate oxide contamination.
- PN junction contamination.
- Failure of metal and polysilicon interconnects.

Some of the possible mechanisms for these failure modes include:

- Chemical attack causing removal of or openings in the insulators.
- Chemical attack causing structural changes can that lead to mechanical failures.
- Condensation of water, mobile ions, and other biochemicals along interfacial planes.
- Dissolution of coatings into the body fluids.
- Electrochemical reactions of insulators leading to dissolution into body fluids.
- Electrochemical corrosion of the silicon substrate.
- Diffusion of water and mobile ions into the gate oxide regions altering thresholds.
- Diffusion of water and mobile ions into PN junctions causing leakage currents.
- Electrochemical dissolution/oxidation of metals and polysilicon.

The global goal of the Insulating Biomaterials contract was to identify or develop methods and materials for encapsulation and protection of implantable assemblies. As the work has progressed, many test devices are lasting very long times and show no trend in degradation. By heating the samples, it may be possible to accelerate the temperature dependent degradation processes. All of the above possible failure mechanisms are almost certainly temperature dependent since they depend on chemical kinetics. However, competing repair mechanisms, and film or coating tensile/compression stresses are also temperature dependent. Temperature dependent processes such as these generally exhibit an exponential relationship and

can be characterized as having an activation energy. The higher the activation energy, the higher the temperature needs to be to achieve a specific reaction rate. Also, the higher the activation energy, the more rapidly a process can be accelerated by increasing the temperature.

It is difficult to have predictive confidence in temperature accelerated data because of the uncertainties inherent in such testing. Without knowing all of the processes that are in effect, and knowing the activation energies of these processes, it is very possible that erroneous conclusions will be made regarding the projected longevity of a device. For example, consider a fictitious material used to encapsulate the bond area of an integrated circuit. Let's assume that the reaction rate for breaking bonds to the surface is lower than the reaction rate for formation of bonds to the surface at room temperature. Also assume that this difference is due to a difference in activation energy, where the activation energy for forming the bonds to the surface is lower than the activation energy for breaking bonds with the surface. If the devices are then heated to accelerate reaction processes, it is possible that the rate curves will in fact cross, and the bond-breaking mechanism will begin to dominate the overall reaction. A graph of this possible scenario is shown in Figure 1. If temperatures above ~60^{O}C were chosen for acceleration, the conclusion could be that the encapsulant was not suitable for the application, even though the actual use temperature would be 37^{O}C where surface bonding dominated over bond breakage. Of course the opposite error could be made. Assume bond breakage initially dominated, but was so slow that the effects could not be seen for several years. Temperature acceleration could cause bond formation to dominate indicating that the material should last indefinitely. However, if the use temperature was 37^{O}C, devices could fail sooner than predicted.

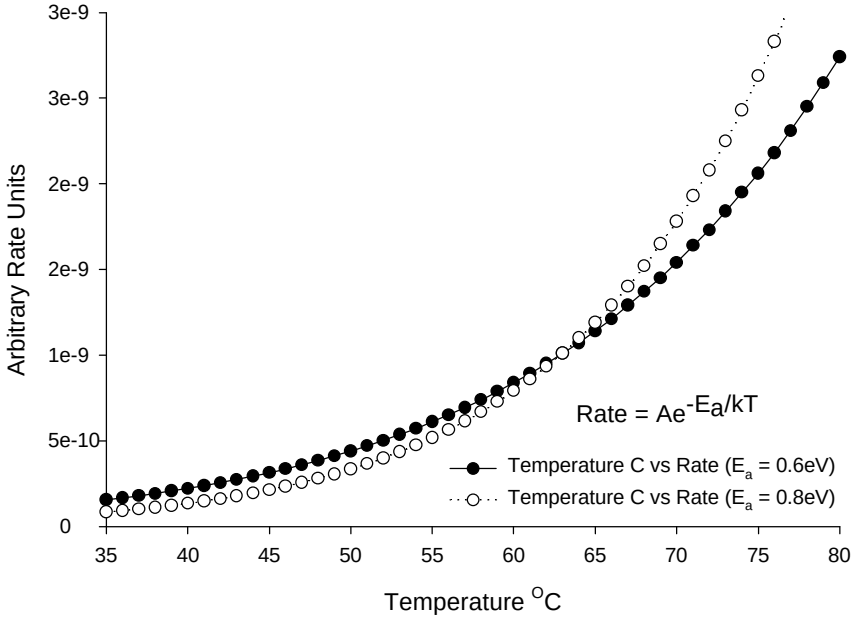


Figure 1: Possible change of dominant reaction rate during thermally accelerated testing.

In spite of these shortcomings, however, accelerated testing may be a useful tool to identify possible problems that can then be further investigated. Another form of accelerated testing is to devise highly sensitive test devices and instrumentation that can detect minute changes in the material or structure being tested. Since the electrical properties are of greatest significance, most of this work has focused on electrical measurement techniques. Inter-Digitated Electrodes (IDEs) provide sensitive measures of surface resistivity at the interface between an encapsulant and device surface. Typically, they are designed as alternating metal traces to provide voltage bias and current sensing. If the total length of the traces is long (~10cm), and the spacing between traces is very small (~0.002cm) the surface resistivity readings in ohms per square will be magnified by ~5,000. Lead wire insulation measurements are taken on as long of lengths of wire as possible to maximize the area under test. Surface coating bulk properties are measured using very thin films with as large of surface area as practical. Integrated circuit elements under test are similarly constructed, though scaled in overall size.

Development of highly sensitive measurement techniques also serves to provide early detection of small changes in device properties. Low noise, low leakage current commercial electrometers were initially used for these measurements. Voltage sweeps were used to create current-voltage data sets that could be fit with linear regression lines. Non-linearities could be detected and used to indicate the presence of electrochemical activity. This system can reliably measure resistances up to 1E15Ω. However, these are very expensive and require use of very high isolation resistance relays for switching to multiplex the measurements. Only one test jar at a time could be measured with this system, and a single set of measurements required several days to complete. A 384 channel electrometer system was implemented during this contract to provide measurements of all devices every 40 hours or so. This opened the way for setting up measurements of devices at different temperatures in addition to simply expanding the number of devices under test.

To keep devices at elevated temperatures, “long tubes” (long screw capped test tubes) were developed that maintain the cap and connections at room temperature while maintaining the devices at 80^{O}C or 90^{O}C. This was necessary because of deterioration of caps and connectors was occurring more rapidly than deterioration of the devices under test. The lower 2 inches or so of the long tubes is placed in a temperature controlled aluminum block. Devices are assembled using long Teflon® insulated wires with silicone insulation over the solder joint. Solder joints of various types have been under soak for many years with silicone insulation and have exhibited no loss of conductivity for lead-tin or lead-tin-silver joints. A Teflon® and silicone diaphragm is used to seal the top of the test tube to minimize water loss.

Routine resistivity measurements consist of stepping the voltage from 0 to 5 to –5 to 0 in 1 volt increments, and from 0 to 0.5 to –0.5 to 0 in 0.1 volt increments. By using two voltage increments, the dynamic range of the system is increased by 10 for linear resistances. After a 60 minute settling time, samples are acquired and averaged from the data acquisition board. At the end of the voltage sweep, linear regression fits are used to compute the slope of the I-V characteristic which is equivalent to the resistance

of the insulator under test. Open circuit measurements, or measurements of devices under soak at 37^{O}C are limited to about 1E15Ω sensitivity. Elevated temperature measurements, however, are limited to about 1E14Ω by excess noise. The noise of the elevated temperature soak tubes comes from the electrical charge noise of the water droplets condensing in the long tubes and falling back into the reservoir which causes significant charge re-distributions. Each sweep cycle requires about 40 hours to complete.

Wire Insulation

Commercially available wire was typically wound onto 5mm diameter spools in lengths of up to 60cm and then immersed in saline at the bottom of long tubes for accelerated testing. Experimental coatings from the CVD reactors were on relatively short wires and required special assembly techniques to avoid damage to the sometimes fragile coatings. In addition, wire joints had to be carefully assembled to avoid formation of parasitic leakage pathways.

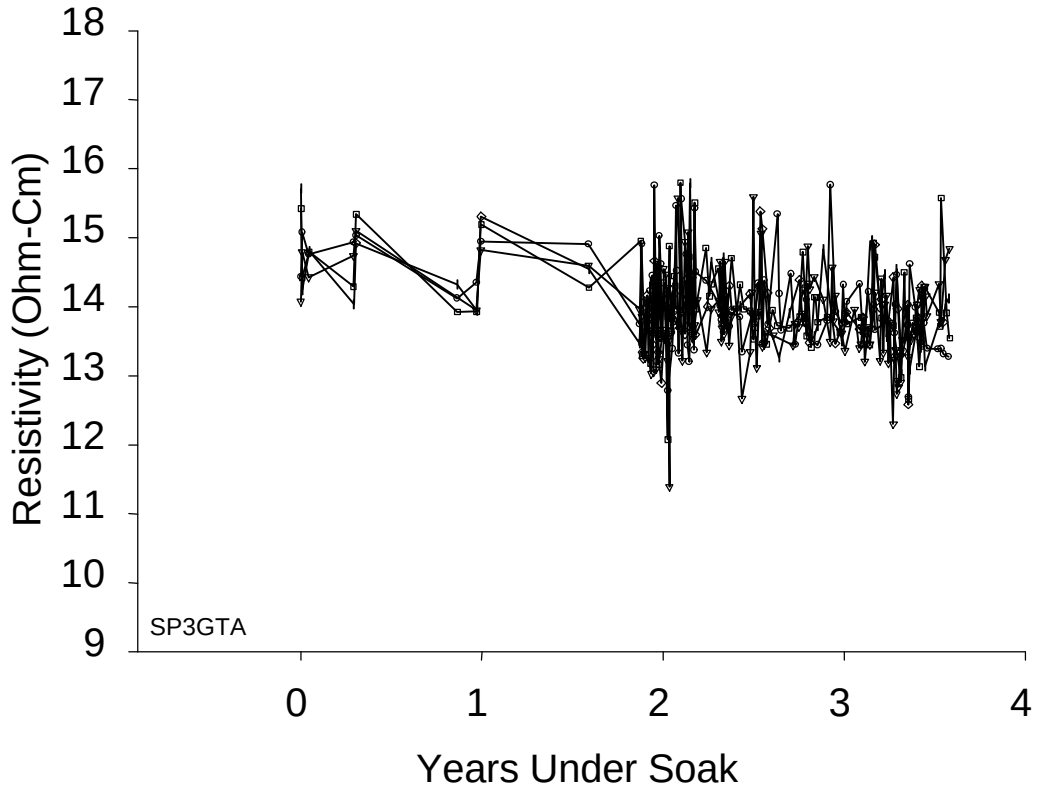


Figure 2: Example of PFA Teflon® insulated 3 mil diameter gold wire from AM-Systems soaked at 90^{O}C in saline for over 3 years in 90^{O}C saline. Approximate area of insulator was 0.7cm^2 with a thickness of approximately 18μm. The corresponding resistivity is approximately 5E16. (Vertical axis is Log Scale).

By far, the most reliable wire tested was PFA Teflon® coated 3 mil wire from AM-Systems. As shown in Figure 2, the raw resistance readings were holding at about 1E14Ω or so. These measurements were taken at 90^{O}C. If we attribute all of the

leakage currents to the wire insulation, the resistivity would be approximately 1E17Ω-cm. Smaller wire diameters were not nearly as reliable as the 0.003" diameter wires. However, failures generally occurred within seconds to hours after immersion indicating that pre-existing defects were to blame for the loss of insulative properties.

While it is generally known that Parylene films tend to "craze" crack when exposed to high humidity environments, Parylene has been used extensively for medical implants, though mostly as a secondary barrier within a welded titanium canister for the pacemaker industry. Experimentally, Parylene has been used for insulation of electrodes and wires for chronic implant assemblies by NIH research scientists developing visual prostheses. Because of the continuing interest in this material, Parylene from Bioelectric Corporation was also tested in low temperature saline soak. 4 of the test wires were 2mil diameter 316lvm stainless steel and 4 were 1mil diameter silver plated copper wire. All test samples were coated with approximately 12μm of Parylene-C. To avoid mechanical stresses on the films, the wires were carefully handled to avoid bending, and were placed in 3" diameter, 3" high test jars to minimize static bending. The resultant loops were approximately 2.5" in diameter and hung freely in saline. Measurement results are summarized in Figure 3. One stainless steel wire in each jar showed open circuit during continuity measurements, possibly due to faulty solder joints. Data for the first two years was eliminated because it was measured using an incorrectly wired adapter. The first data point was re-constructed to illustrate the time that these samples were under test. As can be seen from the data, these Parylene samples performed remarkably well. Additional samples are being procured for testing wrapped on standard 1cm diameter mandrels and soaked in saline at 90°C.

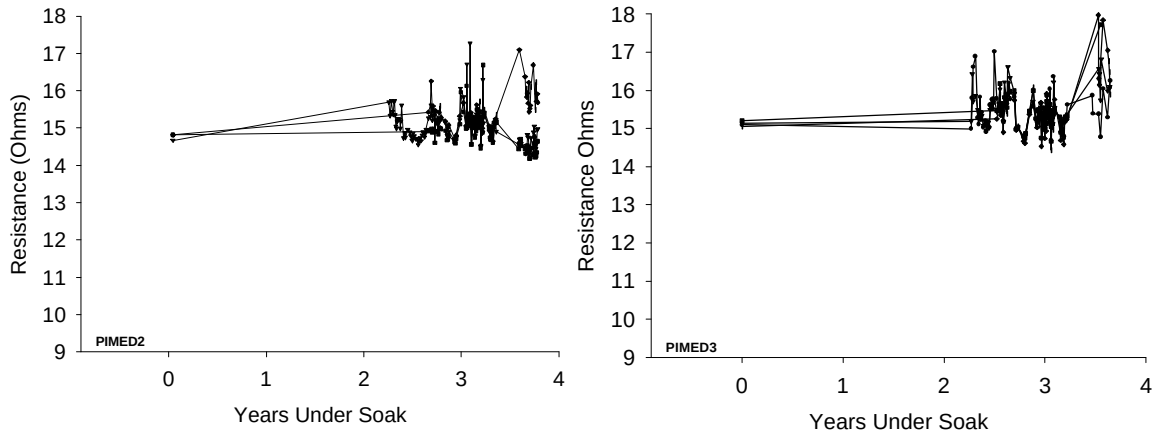


Figure 3: Summary data from 2 sets of Parylene-C coated wires. (Vertical axis is Log Scale).

Another promising new wire coating tested during this contract was "BioKote" provided by John Swanson at BioElectric Corporation. This material is a polyolefin that may be relatively inert. Initial tests were performed on 1mil diameter 316lvm stainless steel wire coated with approximately 20μm of BioKote. Two of the wire samples failed within the first 6 months under test but two other samples only began showing significant

signs of deterioration after 2 years under 37°C continuous soak testing. In view of these results, this particular wire coating is not of great interest for the chronic applications.

By inference from triple track testing discussed below, silicone would also make a high quality wire coating if it could be coated onto small diameter wires. CVD coatings on fine wires have recently been accomplished but soak data is not yet available for evaluation.

Micro-Ribbon Structures

We have been working with the University of Michigan in an effort to define a temporary solution to the problem of interconnecting between the head mounted connectors and the intra-cortical electrode arrays. One aspect of this work was to develop thin film coatings from CVD reactors that are suitable for strengthening, protecting and shaping silicon micro-ribbon cables produced at the University of Michigan. While these coatings are now possible, fixturing of the micro-ribbons is very difficult, and use of the micro-ribbons for long distances makes fabrication very difficult as well as expensive. In collaboration with the University of Michigan, alternative solutions to the interconnect problem are being investigated. Polyimide based ribbon cables have been in existence for many years. Our testing of polyimide wire insulation showed that the insulator failed within 8 months or so in room temperature saline due to cracking. Apparently this was due to residual stresses in the coatings acting on partially hydrolyzed polyimide. However, without stresses acting on the films, the results could have been different. In any event, an 8 month solution to the electrode array interconnect problem would be welcomed.

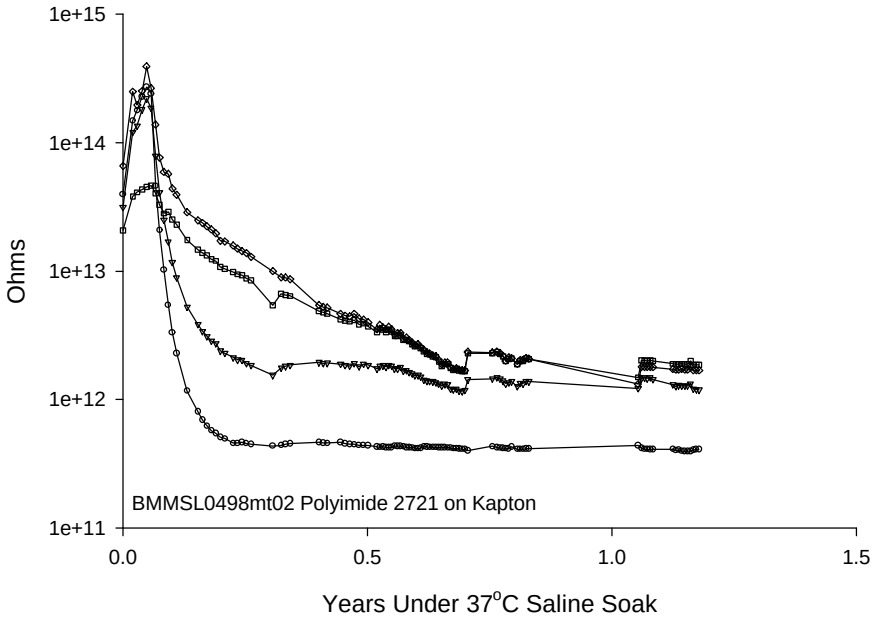


Figure 4: Soak results of Dupont PI2721 on a 2 mil Kapton substrate patterned with gold interdigitated electrodes by NCSU. (Vertical axis is Log Scale).

Large scale model triple track arrays fabricated with a variety of commercial Kapton flex circuit approaches failed apparently due to attack of the acrylic or epoxy adhesive/polyimide interface, incomplete removal of the copper between traces, or contamination prior to assembly. Several epoxies (Epotek 353ND, 377, and 301) effectively insulated copper traces on bare polyimide (Kapton), but it was not clear that this could be used to fabricate a flexible, long lasting interconnect. Jamie Hetke from the University of Michigan had some test ribbons fabricated by Dynaflex that performed fairly well for a short time, but then rapidly failed as apparently the acrylic interface failed.

Troy Nagle and Jason Fiering at North Carolina State University fabricated some interdigitated electrodes using Kapton and 5 different insulators including 2 types of polyimide. All failed except one Kapton structure that was coated with Dupont PI2721. All four test devices fabricated with these materials have been under test for over one year and are doing quite well as shown in Figure 4. This structure holds considerable promise for the short term interconnect needed as a bridge between head connectors and intracortical electrode arrays.

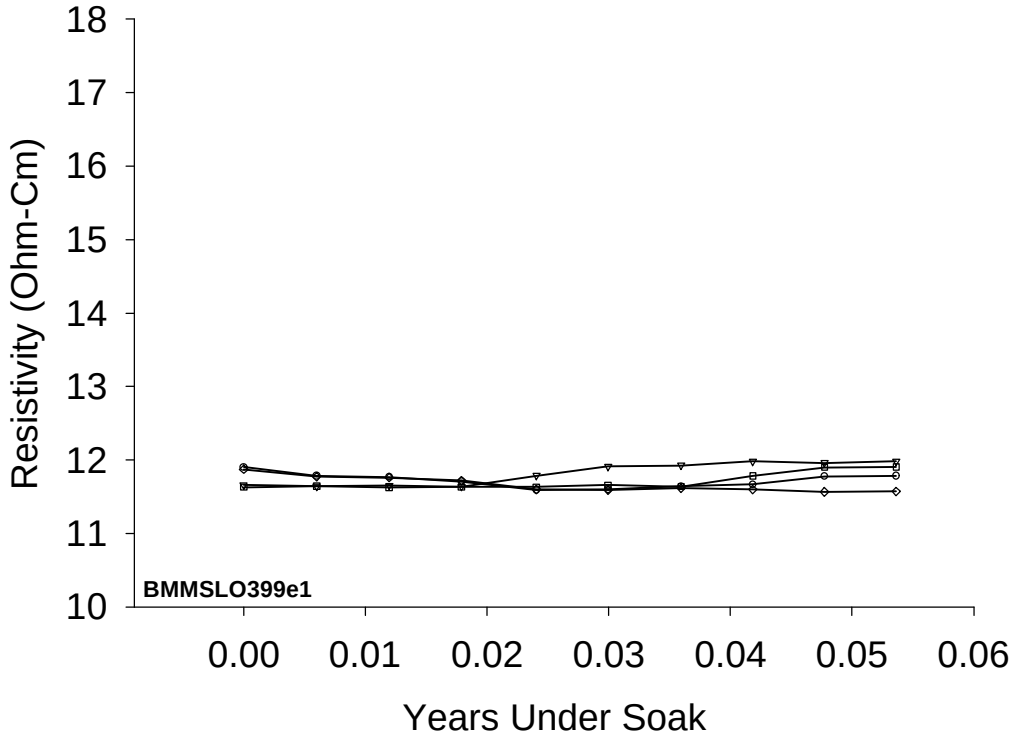


Figure 5: IDEs from NCSU fabricated with Upilex substrate material and Dupont PI2721. In addition, an NCSU proprietary moisture barrier material ("A-coat") was applied to these. (Vertical axis is Log Scale).

Addition samples were recently placed under long term soak at 37^{O}C and early results are shown in Figure 5. It is noteworthy that these samples appear to be more stable in behavior than the pure polyimide assemblies shown in Figure 4.

Jamie Hetke of the CNCT at the University of Michigan designed a ribbon cable and connector assembly for the NCSU Kapton technology. Jason Fiering at NCSU fabricated these structures. Jamie assembled them with Omnetics connectors and provided four samples for saline soak evaluation. These were installed in jars and placed under test with the bottom of the connectors exposed to the saline as well as the ribbon interconnects and bond area. The bond area and Omnetics attachment was protected with Epoxy Technology 353NDT. Silver epoxy was used to attach the omnetics connectors to the gold bond pads of the ribbon cable. The cables were approximately 1.5cm long, with 3 mil wide traces, spaced 3 mil apart. The bond area traces were 4 mils wide spaced 2 mil apart.

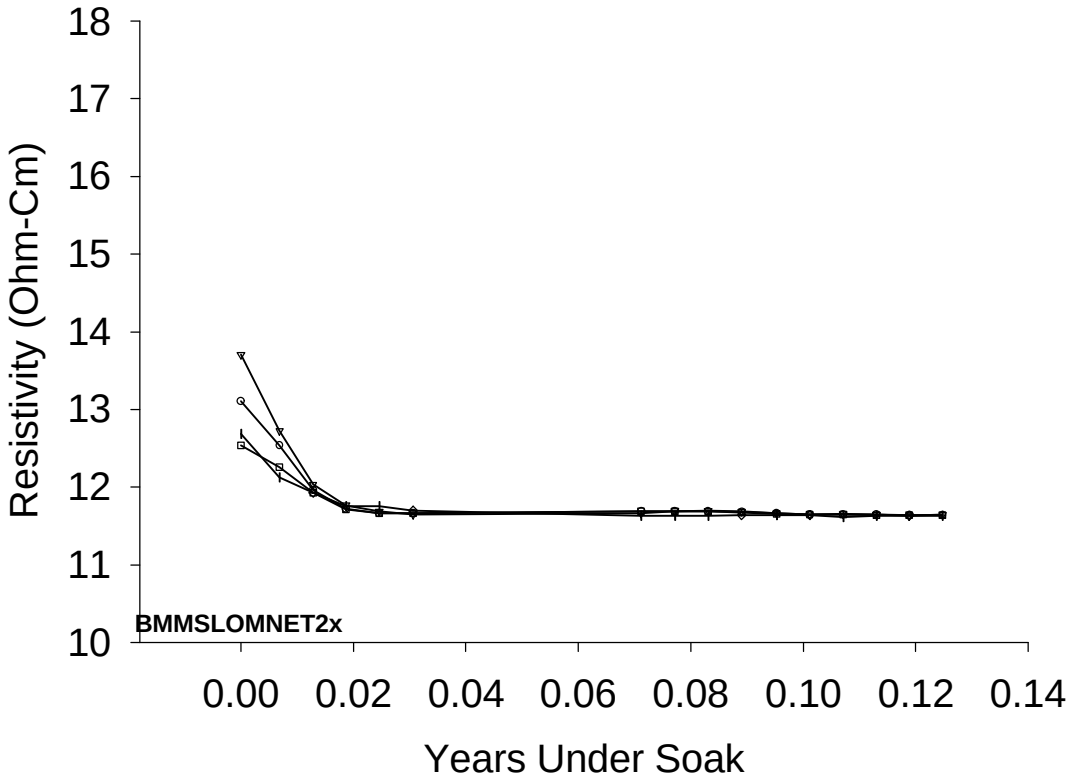


Figure 6: Short term 37^{O}C saline soak data for Omnetics Connector – Kapton- PI2721 assembly with Epotek 353NDT coated bond pad area. (Vertical axis is Log Scale).

Early soak test results (Figure 1) indicate that these assemblies are functioning quite well, and will likely be robust interconnects for short term chronic animal implantation.

Surface Encapsulation

Triple track or Inter-Digitated Electrode devices have become the main test devices for evaluation of surface encapsulation materials. These devices consist of silicon dioxide surfaces with two voltage setting electrodes on either side of a current sensing electrode. The electrodes are typically spaced 20μm apart and are 10μm wide (30μm pitch). They are serpentined to provide long lenghts which result in about 1E-4 - 1E-5 squares of surface resistivity. These devices and the associated I-V measurement instrumentation are capable of sensing surface resistivities on the order of 1E18Ω/ .

To put this in perspective, if a 10 volt bias were applied to two 10μm long traces with 10μm between, 1E-17amperes (10attoAmperes or 10aA) would flow. For discussion, assume that the actual pathway being measured is 1000Å wide and high, and that every electron contributes to growth of a metal (assume platinum) dendrite. Platinum atoms are roughly 195g/mole/(6.023E23 atoms/mole x 21.45g/cm^3) = 15 A^3/atom. Since the volume of the dendrite would be about 1E5Å x 1000Å x 1000Å = 1E11Å^3, roughly 1E10 atoms would be required, or a total charge transfer of 1e10 electrons or 1nCoulomb (nC). A current of 10aA flows 10aC/sec. At that rate, this assumed dendrite would form in a little more than 3 years. Once formed, the resulting shunt resistance of the dendrite would be approximately 10μΩ-cm x 1E-3cm/1E-10cm^2= 100Ω if bulk electronic properties applied to the dendrite. Intermittent behavior would be expected because the current density through such a dendrite would be very large once a bridge was formed. Very high current densities could cause electromigration of the atoms resulting in an open circuit which would then fill back in over time.

While it is unlikely that calculations such as these can be precise, they at least provide perspective on what a worst case scenario might be for a leakage current of 10aA and serve to illustrate some of the uncertainties involved in interpretation of the data.

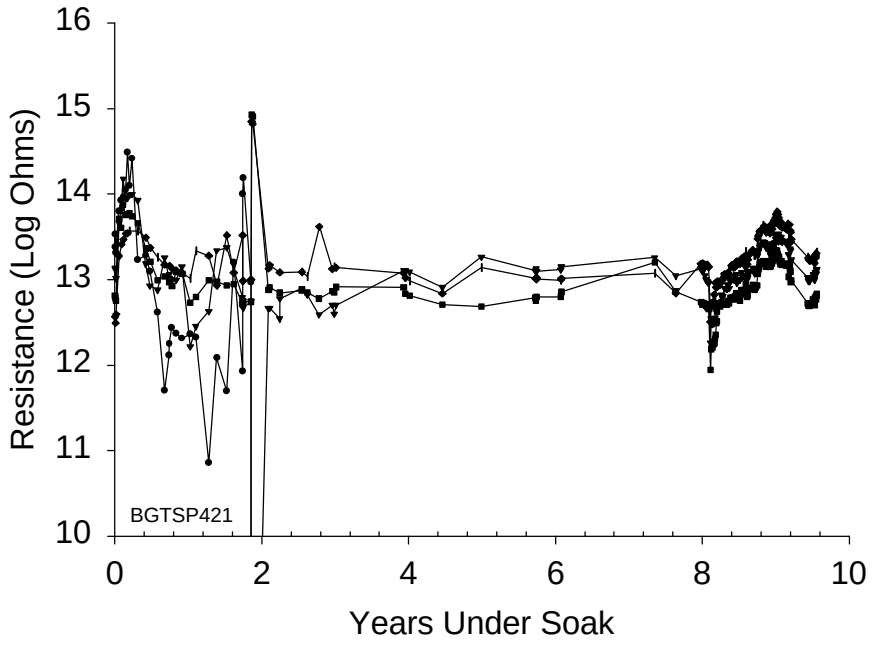


Figure 7: Raw resistance measurements from first bond chip assembled with Dow Corning MDX-4-4210. Surface resistivity in ohms/square is approximately 10^4 times the raw resistances.

Measurements begun many years ago with “Bond Chip” assemblies included 4 sets of IDEs concentric about a set of bonding test structures and a polysilicon resistor. The first test devices were all encapsulated with epoxies that had been used for long term implant work. After a few weeks, all devices failed precipitously. Generally, there was delamination of the epoxies from the surface of the bond chip. The observed

delamination may have been due to hydrolysis of carbon-oxygen-silicon bonds that must form between the epoxy and silicon dioxide surface for bonding to occur.

Silicones, however, bond to silicon dioxide to form silicon-oxygen-silicon linkages which are relatively stable. Figure 7 shows long term soak test results from one of the better silicone encapsulated assemblies. This device was the first silicone sample assembled using Dow Corning MDX-4-4210 platinum catalyzed silicone. Raw resistance data is shown since the conversion to ohms/square requires assumptions about the partitioning of the currents to bulk and surface pathways. If all of the current flowed through the surface pathway, the surface resistivity would be about 10^4 times the raw readings based on the width to length ratio of the spacing between metal traces. After 7.5 years the device was moved to a multichannel electrometer test system that measures each device once every 2-3 days depending on how many devices are under test. It is noteworthy that the inner set of IDEs for the device whose data is shown in Figure 7 failed after about 2 years, but the outer 3 adjacent sets all continued to maintain a high resistance level. In addition, the inner resistance measurements of ball bond to bond pad, bond pad to polysilicon, and polysilicon resistances have also held steady over the decade that this device has been under test.

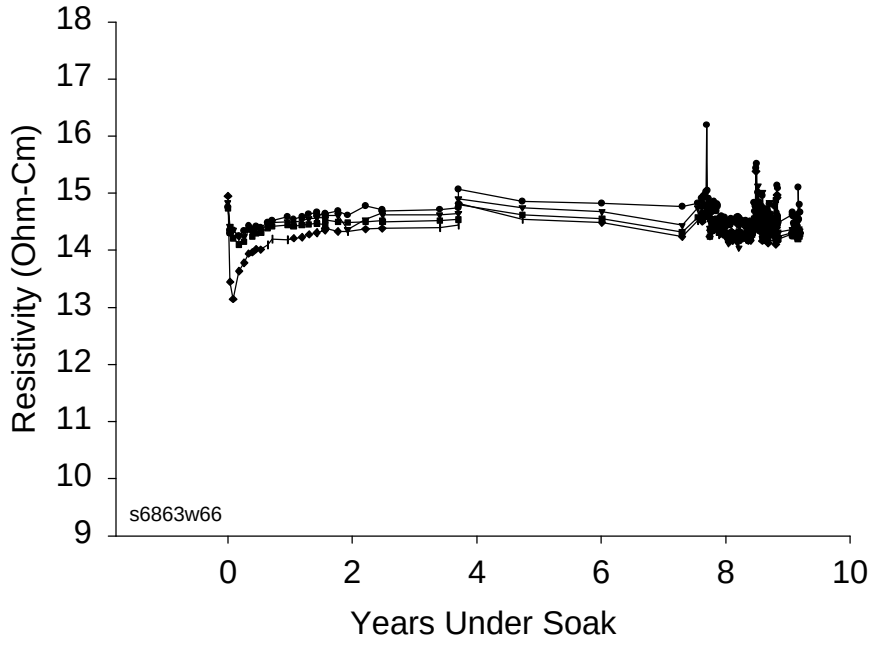


Figure 8: Long term results from IDEs on a Bond Chip encapsulated with experimental silicone material from Dow Corning. (Vertical axis is Log Scale).

Not all devices tested as well as this device, but most have. Of the 7 samples assembled with MDX-4-4210, 4 are still under test. One failed due to shrinkage of epoxy used to overcoat the leads and connector. The two other failures were probably attributable to contamination during the wire bonding phase of the assembly. Other silicones have performed as well as or better than the MDX-4-4210 material. Analogs of the Dow Corning MDX-4-4210 material such as Huls PEM25A, Factor-II-2186, Applied Silicone LSR-30, and Nusil MED-4211 have all performed well when the

substrates are properly cleaned and processed. In addition, some experimental materials from Dow Corning have also performed very well. Figure 8 shows summary data from the IDEs on a bond chip encapsulated with one of the experimental silicones. After an initial transient often observed with these assemblies, the resistances were remarkably stable for nearly a decade so far. Laboratory moves, and changes in instrumentation accounted for variations in the observed readings at times. For comparison, Figure 9 shows long term soak data for a bond chip assembled as all the others, but with the interconnecting wires left just above the bond pads rather than actually bonded to the IDEs. All leakage currents from this assembly would be attributable to bulk conductivity of the encapsulant, wire insulation, connector, and measurement system. As can be seen in Figure 9, the control resistance readings are similar to the experimental resistance readings shown in Figure 8 indicating that the surface is indeed passivated by these coatings.

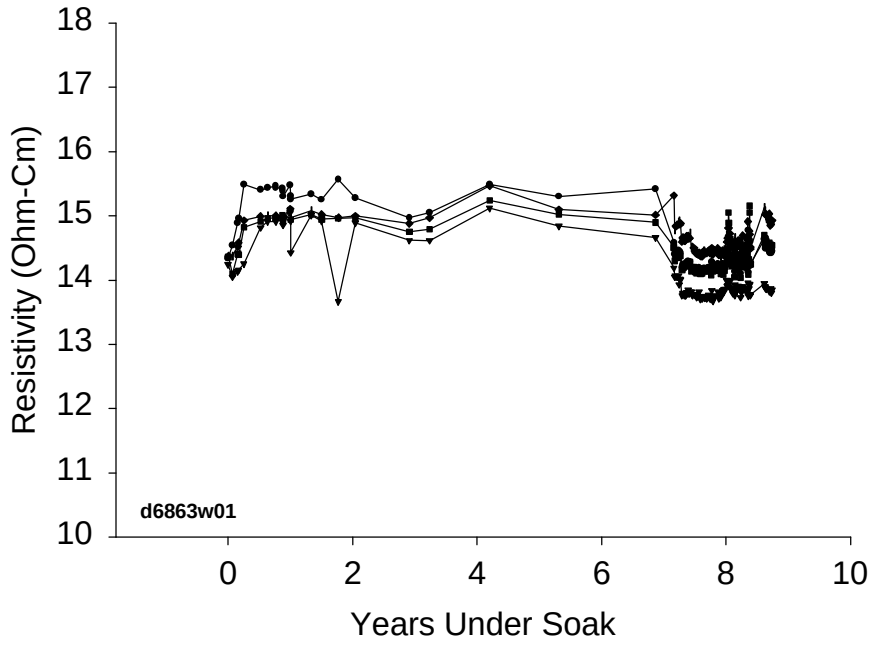


Figure 9: Long term soak data for device where the bond chip was not actually bonded to the lead wires thereby providing baseline data for resistances in the system due to other sources than bond chip surface leakage currents. (Vertical axis is Log Scale).

Occasionally we have tested silicones that do not perform well. Nusil MED-6210 was thought to be an excellent material until test results showed consistent failures after short times. While not completely understood, the failures were thought to be due to the use of silicone resin filler material rather than the fumed silica material used for the other silicones tested.

In addition to the IDEs on the bond chips, several resistor test structures were also included. Possible resistance measurements included a polysilicon resistor, metal to poly contact, and bond wire to bond pad contact resistance. Each device was connected to allow use of four point resistance measurements which was particularly

important for the low value resistances. In addition, four point measurements allowed direct measurement of the polysilicon independent of contact and bond wire resistance.

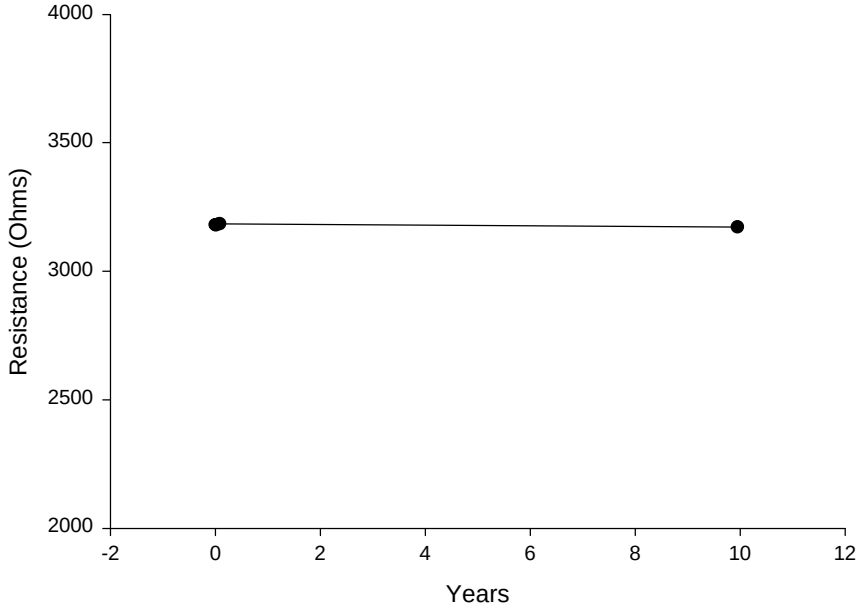


Figure 10: Polysilicon resistance for BGTSP421 bond chip coated with MDX-4-4210. Absence of measurements was due to a measurement program bug. Newest measurement is about 10Ω less than original set, possibly due to slightly different temperature.

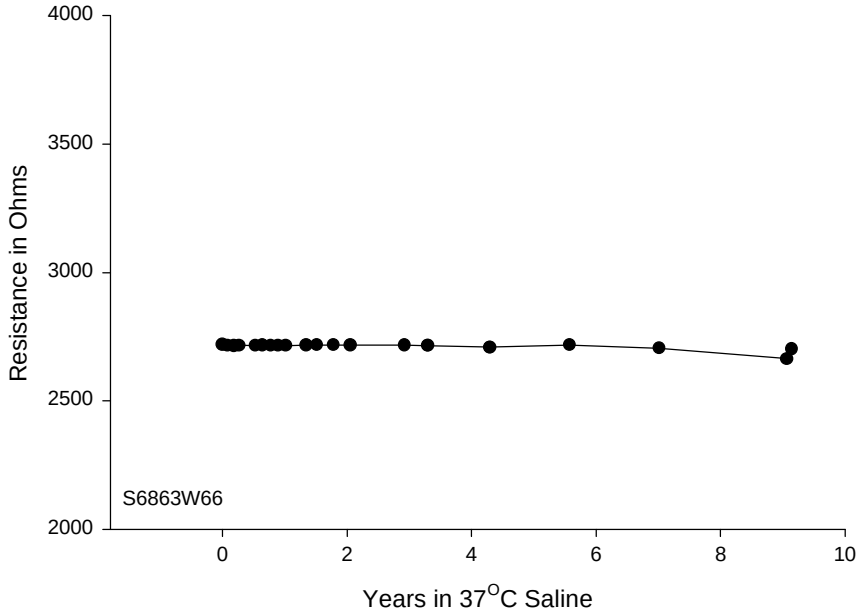


Figure 11: Polysilicon resistance for bond chip coated with Dow Corning experimental encapsulant x6863. Dip in curve at end is due to measurements made at different temperatures (TCR_{polysi}~ 0.13% from these measurements).

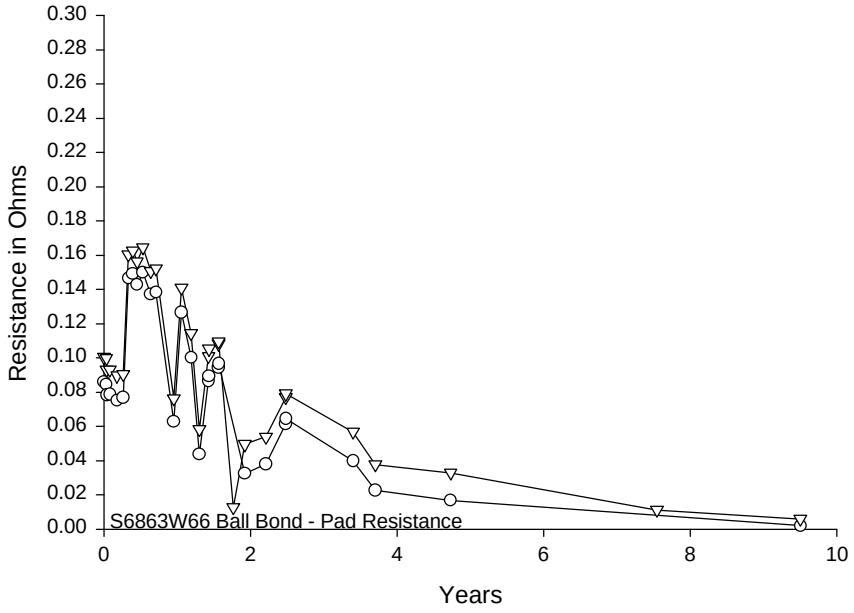


Figure 12: Ball bond to bond pad resistance for bond chip coated with Dow Corning experimental silicone x6863.

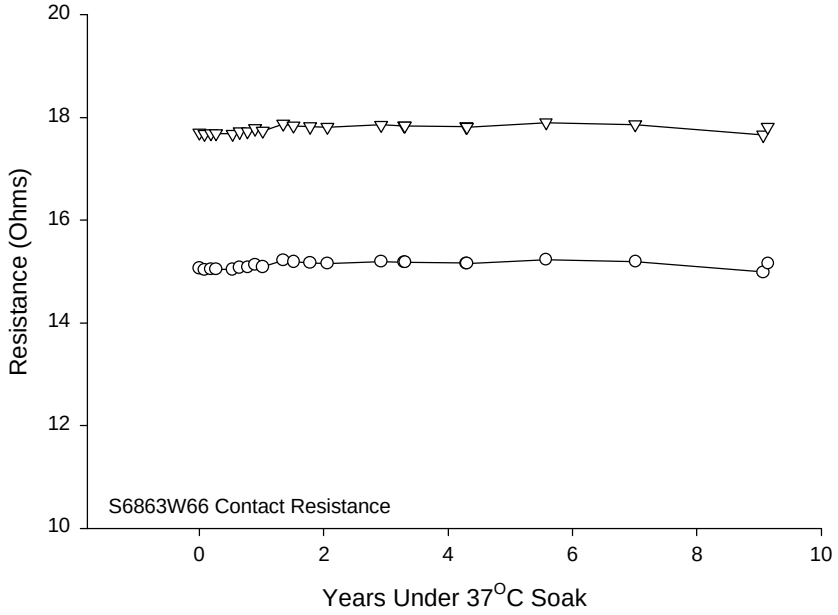


Figure 13: Contact resistances for bond chip coated with Dow Corning experimental silicone x6863. Dip in curve at end is due to measurements made at different temperatures (TCR_{polysi}~ 0.13% from these measurements).

In general, the low resistance devices on the bond chips show little change. Because the measurment system was changed during year 9, the slight downward trends observed for contact and polysilicon measurements may have been due to the different measurement technique. Ball bond resistance seemed to decline substantially from approximately 0.1Ω down to 0.01Ω. The cause of this is unknown but may be due to electromigration solidifying the bonds.

In-Vivo Evaluations

Over 40 animals were implanted with a variety of test devices placed subcutaneously or subdurally. Biasing battery capsules were mounted on the percutaneous connectors and worked well. Unfortunately, most of the soft tissue percutaneous connectors marsupialized within about 8 months or less and were destroyed when the animals chewed the implanted devices. However, several devices were implanted under the paraspinal fascia in an effort to block the epithelial downgrowth with the fibrous tendon. This was attempted after it learned from dental literature that fibrous materials were being used successfully to block epithelialization of the roots of teeth following periodontal repairs. These particular devices were successful and have been monitored for over 3 years and are still under test as indicated in Table 1. We have also lost most of the subdural implants due to the animals apparently banging their connectors on the caging when startled. Current results are summarized in Table 1 (results have not significantly changed since then). Hip triple track devices consisted of four interdigitated electrode arrays (IDE arrays) mounted on titanium percutaneous connectors. Of many that were implanted, only two continue to survive for many years. These devices have continuous 6 volt battery voltage applied between the traces of the IDE arrays. Wire loop implants consisted of 1cm long loops of wire implanted subdurally and leading through the skull to a percutaneous connector. Head triple track devices consisted of 2 IDE arrays implanted subdurally with lead wires through the skull to a percutaneous plug. Channels 8 and 10 were not functional in these implants since there were only 2 IDE arrays.

	Channel >		4	6	8	10		
Animal ID	Type	Years	Interdigitated Electrode Ohms				Date Tested	Date Implanted
R4211B	Hip TT	3.6	1.96E+14	3.35E+12	1.36E+11	1.98E+12	12/20/98	07/11/95
R2186B	Hip TT	3.4	<1 E+9	>2 E+14	>2 E+14	>2 E+14	12/20/98	10/03/95
R3PITA	Wire Loops	1.7	4.91E+13	2.27E+13	1.32E+13	1.78E+13	12/20/98	05/20/97
R2PT3A	Wire Loops	1.7	1.96E+14	6.81E+13	5.27E+13	<1 E+9	12/20/98	05/30/97
R4220B	Head TT	1.5	1.35E+11	>2 E+14	NA	NA	12/20/98	08/05/97
R4220C	Head TT	1.5	>2 E+14	2.04E+14	NA	NA	12/20/98	08/07/97
R2500C	Head TT	1.4	9.82E+12	<1 E+9	NA	NA	12/20/98	10/06/97

Table 1: Summary of surviving subcutaneous triple track implants over the hip (Hip TT) sub-dural wire loop implants (Wire Loops), and sub-dural triple track implants (Head TT) in rabbits.

It is impressive to us that the silicone encapsulated triple tracks have survived for over 3 years at this point. The silicones used correspond to the animal ID. Implant R4211B was coated with Nusil MED-4211. Implant R2186B was coated with Nusil CF20-2186. Implants R4220B, C were coated with Nusil MED-4220. Implant R2500C was coated with Nusil CV2500, a low volatiles/ultrapure silicone. The R4211B and R2186B implants together have only exhibited one of 8 failures over the 3 year period. The readings indicate a surface resistivity of between 1E16 to 1E18 Ω/sq. The newer head

implants are exhibiting similar performance. The Teflon coated wire loops are also performing in similar fashion to the wire loop tests run in-vitro.

While this table has become far smaller than originally planned, we are obtaining useful animal data. The totally implantable, high sensitivity, multichannel electrometers that transmit data across the skin with no percutaneous connectors will solve all of the issues that have thus far limited this portion of the insulating biomaterials contract. These devices will be very similar to the PassChip described above, and will perhaps revolutionize our ability to gather this critical data.

Mechanical Properties of Materials

One widely accepted theory of silicone degradation [Noll, Silicone Chemistry1968] is that it is caused by a pair of competing reactions. One process is the formation of additional cross linkages which results in stiffening and hardening of the material. Tensile strength is increased generally. The second process is the de-polymerization of the material which results in softening the material. Which process dominates depends to a large extent on the conditions of aging. In the presence of oxygen and the absence of water, and particularly at elevated temperatures, additional cross linkages are formed by oxidation of the organic constituents resulting in hardening. In the absence of oxygen and the presence of water, hydrolysis of cross linkages and chain scission may occur resulting in softening. The stability of the material at the beginning of the aging process may also impact the outcome of these competing reactions. Hydrolysis of cross linkages is a reversible process. If the molecules are hindered from physically moving apart, then the cross linkages can readily repair. Thus, a material that is initially more cross linked may in fact be more stable, or a material that becomes more cross linked in the presence of oxygen may become more stable with time. In addition to the amount of cross linkages designed into the material, the number of cross links is also a strong function of the cure schedule over some temperature range.

To begin to understand these issues for the materials we are evaluating, a small matrix of pull tests of samples of a representative silicone (CF20-2186 from Nusil) were recently begun. Once we are sure we have the methodology well defined, a larger matrix will be explored if indicated. Sixteen 20cm long rods of CF20-2186 silicone were cast using 2mm diameter Teflon® tubing as a mold. Curing time was 3 hours for all cycles. All rods were cured at 50°C. Four of these rods received an additional air cure of 100°C. Four others received an air cure of 150°C. The remaining four received and additional cure of 200°C. All were then tied into loops using "fisherman's knots" to secure the ends. The resulting o-ring structures were then pull tested on a simple pull system that used a sensitive computer interfaced Mettler® balance for measurements. Measurements consisted of alternately stretching and relaxing the rings using 1/4" diameter stainless steel rods that were moved by a micro-stepping linear actuator. The resulting slope of the force-displacement curves were then used to compute Young's modulus.

One loop from each cure schedule group was placed in one of four environmental conditions: 1) 90°C saline, 2) 80°C saline, 3) 26°C saline, and 4) 26°C air.

Periodically the loops were withdrawn from their aging environments and pull cycled. As shown in Figure 14, there appears to be a general stiffening of the material with time that is accelerated by elevated temperature saline soaks. Apparently there is a non-linear effect of cure temperature on the elasticity of the silicones that may be significant for applications. While coarse, it appears that the Dow Corning recommended cure schedule of over 150°C for over 3 hours has merit since the two samples cured at or below 100°C are clearly less stiff than the samples cured at or over 150°C. It is noteworthy that none of the samples became less stiff with time. This may indicate that even when cured at 50°C, the strucuture of the silicone is stable enough to ensure that cross-linking will be the dominant long term reaction. The method appears to be useful and may define proper cure schedules for silicones used as insulating biomaterials. In-vitro studies should begin next contract.

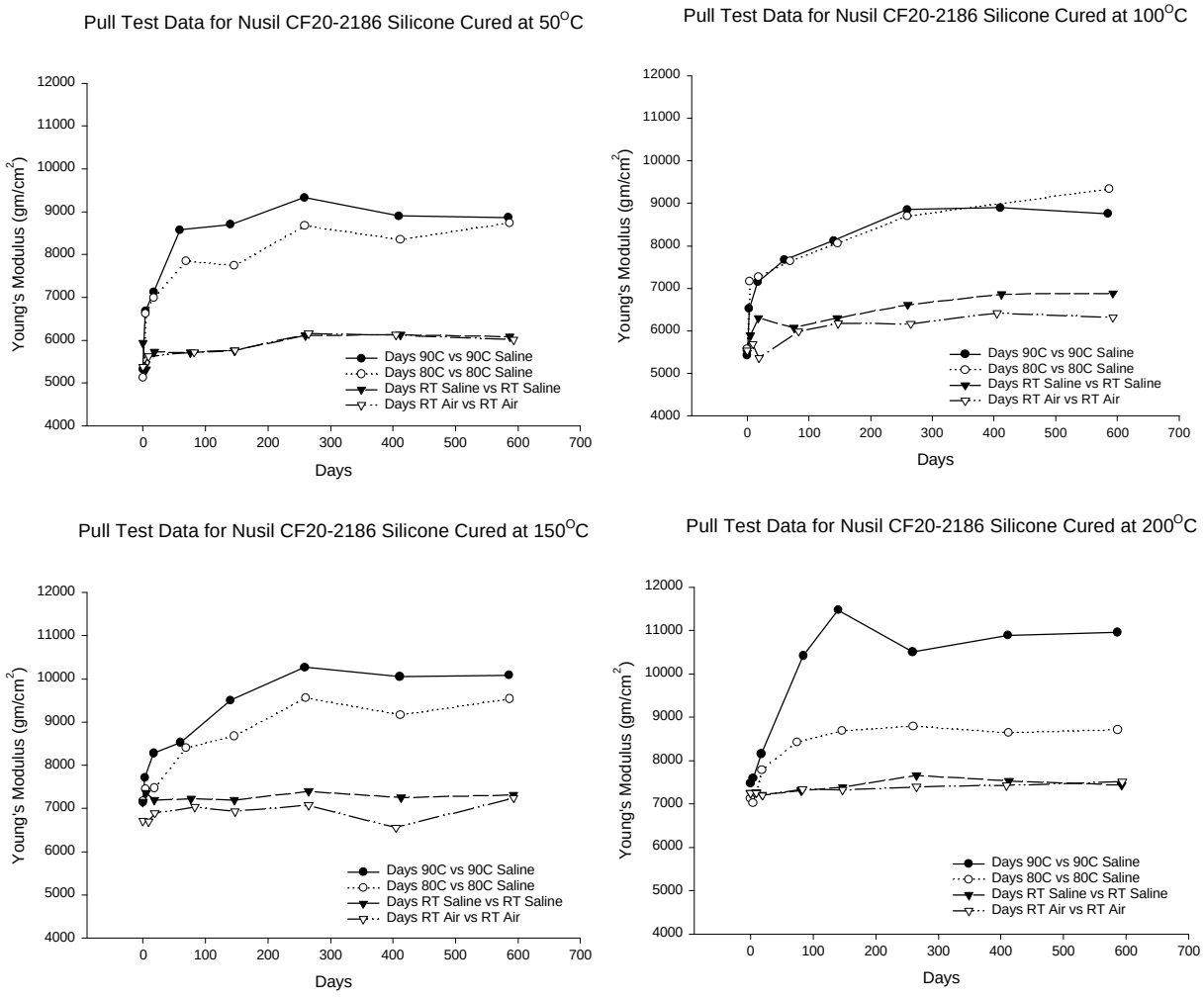


Figure 14: Young's modulus versus aging in days under various conditions for samples of Nusil CF20-2186 cured under various conditions.

Substrate Corrosion

Since we began testing silicon nitride as a surface coating, we noticed that a very thin coating of silicone prevented dissolution of the silicon nitride. Since then a variety of surface tests were performed including implantation of double polished silicon pieces coated on one side by silicone. The original intent of this was to allow infiltration of biochemicals which could then be detected by differential FTIR spectroscopy.

However, removal of the silicon pieces 6 months later, revealed that the unprotected backside of the silicon had corroded to such an extent that the FTIR measurements could not be completed. This may indicate that silicon must be protected in some way to avoid corrosion. Since the University of Michigan program's devices had no protection for the underlying silicon substrate, this finding was significant. However, corrosion of UM devices had not been reported, so to determine if the P^+ substrates were somehow inherently corrosion proof, some example devices were obtained for testing. Devices were implanted subcutaneously and in the subdural space of a New Zealand rabbit and left in place for nearly one year. None of the devices showed any evidence whatsoever of corrosion of the substrate. In fact, the micro-pattern left by the boron etch stop process remained as well. There was some evidence of corrosion of the front surface of the structure evidenced by a rainbow effect on the dielectrics that was not previously noted.While this is good news for the current probe technology, the amount of doping required to protect the substrates is not known. Active probe technology from the UM program have lighter doped substrates. Further, depending on etch conditions, it may be that many probes have some or all of their exposed silicon surfaces relatively lightly doped if they come out of the etch too soon. This likely happens as some probes etch out before others. The residual silicon may in fact be etchable when implanted. Future work will attempt to set boundaries for the onset of the corrosion process.

Chip Surface Coating

Thin film ceramics are needed to provide ion and water barriers to protect CMOS integrated circuits under soak conditions. Typically, semiconductor manufacturers rely on silicon nitride for that function. In our ongoing tests, we have found that silicon nitride is susceptible to dissolution when subjected to biased soak conditions. We have made many attempts at defining the limits of this process, and to identify possible alternatives. A new set of test devices that take advantage of the silicon wafer bulk resistance test configuration have been under test and are yielding reliable data. These test structures consist of small silicon wafers that have been coated with the materials shown in Table 2. Wires are attached to the wafer backs and the entire assembly is potted in silicone except for a round window, 6mm in diameter, over the film under test. Four of these are then assembled into long tubes and placed under heated soak conditions at 90°C to accelerate what appears to be a chemical process.

- 1,000A LPCVD silicon nitride on bare silicon.
- 5,000A PECVD silicon nitride on bare silicon.
- 1,000A LPCVD silicon nitride over 1,000A thermal oxide.
- 5,000A PECVD silicon nitride over 1,000A thermal oxide.
- 5,000A LTO deposited oxide over 1,000A LPCVD silicon nitride on bare silicon.
- 5,000A LTO deposited oxide over 5,000A PECVD silicon nitride on bare silicon.
- Bare silicon coated with Nusil CV2500 for a control.

Table 2: Devices under test for evaluation of thin film inorganic dielectrics.

All of the 1,000A LPCVD silicon nitride coatings of bare silicon failed in less than 7 months under ±5 volt continuous IV sweep measurements. Two of the 5,000A PECVD silicon nitride samples failed in approximately 9 months with two surviving for 15 months and are still under test. Similar behavior is being observed for the remainder of the devices listed in Table 2 with the exception of the two types that have 5,000A LTO (Low Temperature Oxide) overcoating the silicon nitride layers. As shown in Figure 15, these two types have all 8 devices surviving for over 15 months and are still under test. This appears to verify the hypothesis that silicon dioxide somehow may stabilize the silicon nitride layer if it is applied to the outer surface. Notably, very thin films of silicone applied to silicon nitride also appear to protect the silicon nitride. Thus it may be that LTO can be used to stabilize silicon nitride which can then be used as a reliable, long term ionic barrier for CMOS circuits.

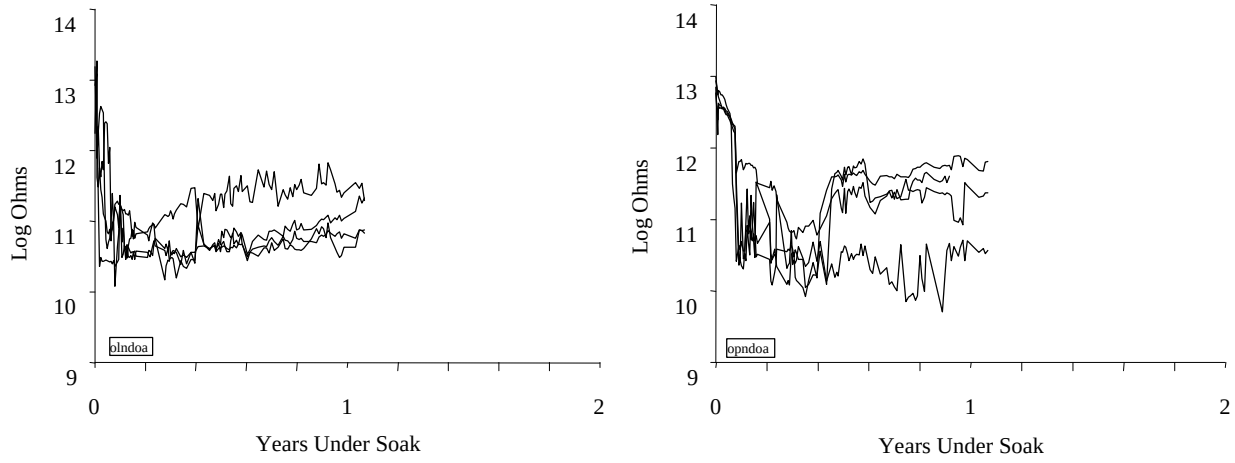


Figure 15: Result of biased soak testing at 90°C for silicon wafers protected with 5,000A of LTO over 1,000A LPCVD silicon nitride (left). 5,000A PECVD silicon nitride (right).

CVD Fluoropolymers

CVD fluoropolymers were tested extensively both as wire coatings and as substrate coatings. While very flexible, conformal coating could be produced the coatings were quite fragile which necessitated special handling. Approximately 30 devices were assembled into soak chambers and evaluated in saline. However, only one device did not de-laminate and did not have included defects. This device has been under test for several years (see Figure 16). While the resistivity is perhaps slightly lower than bulk PTFE, it is still excellent. However, these films do not covalently link with silicon dioxide surfaces and thus may not be suitable for substrate protection. In view of this inherent limitation, the fragile nature of the flexible films, and the option of developing films using silicone chemistry, the research emphasis was shifted to silicones. Fluoropolymer research is continuing, however, mostly funded by commercial sources.

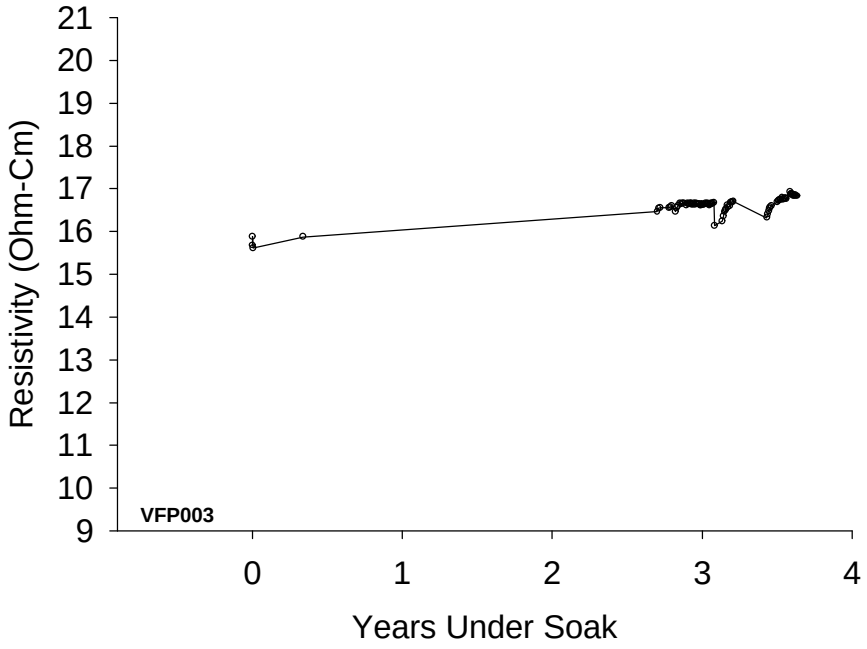


Figure 16: PPECVD fluoropolymer coating on silicon. Film thickness was approximately 10μm. (Vertical axis is Log Scale).

CVD Silicones

Sample	Mode	Ave Ω-cm	% Survival	Years
RSPSLL2	Continuous	1.26E+12	0.75	1.23
RSPSLL3	10/100	2.05E+13	1	1.23
RSPSLL4	100/400	2.22E+13	0.5	1.23
RSPSLL5	Continuous	7.77E+12	1	1.23
RSPSLL6	100/400	1.00E+13	1	1.23
RSPSLL7	10/100	7.19E+13	0.75	1.23
RSPSLL8	100/600	4.67E+13	1	0.90
RSPSLL9	10/250	9.06E+12	0.5	0.90
RSPSLL10	10/60	9.66E+13	0.75	0.90
RSPSLL11	100/400	4.22E+13	1	0.90
RSPSLL12	100/400	5.07E+13	1	0.90
RSPSLL13	10/100	1.95E+14	1	0.90
RSPSLL14	Continuous	3.26E+13	1	0.90
RSPSLL15	100/200	2.19E+13	0.75	0.90
RSPSLL16	10/60	2.02E+13	0.75	0.90
RSPSLL17	50/300	2.85E+13	0.75	0.73
	AVERAGE	2.37E+13	84%	

As of Sept 30, 1999

Table 3: Summary of soak testing results for PPECVD silicone coated silicon pieces.

Squares of semiconductor grade silicon were cleaned and coated with PPECVD silicone films under a variety of conditions. Each deposition resulted in 5 samples, one for thickness measurements and the other four were used for bulk resistivity measurements. Once coated with the PPECVD film, silicone o-rings were glued to the surface of the silicon pieces to delineate an area of 0.28cm^2 to be exposed to saline. Wires were attached to the backside of the silicon pieces using silver epoxy on a freshly scratched surface. All areas other than the test area were then coated with silicone to provide electrical isolation. All four test samples for each deposition type were then immersed in saline at the bottom of a 12” glass test tube which was then heated to 80^{O}C and plugged into the electrometer system. Current-voltage sweeps from –5 volts to +5 volts relative to a platinum ball electrode were run continuously. Table 3 shows current results of this testing. It’s clear that PPECVD silicones are robust films that appear to adhere very well to silicon surfaces. These bulk resistivity readings are somewhat low for high quality silicones (~1e16Ω-cm), but are acceptable. This may be a parameter that can be optimized in the future. There is no striking relationship between the performance of the materials and the deposition parameters.

The failure mode observed in these samples appears to be either defect inclusion or cracking (in the case of continuous mode depositions). PPECVD wires have not yet been fabricated that have the required flexibility.

Pyrolytic silicone depositions from Hot Filament Chemical Vapor Deposition (HFCVD) were also developed and were used to coat 3 mil copper wires with flexible, tough coatings. Of 17 that were coated with approximately 10µm of HFCVD silicone, 13 tested above 5E12Ω for a 1cm immersed section. Several of these samples had previously been pulled into an 800µm diameter loop for evaluation of flexibility. These samples were assembled into long tubes for saline soak testing which is now in progress.

Protection of Integrated Circuits

An integrated circuit test chip was developed to study the effects of implantation on sensitive CMOS integrated circuit elements. This “PassChip” shown in Figure 17 was implemented in MOSIS-Orbit 2µm technology.

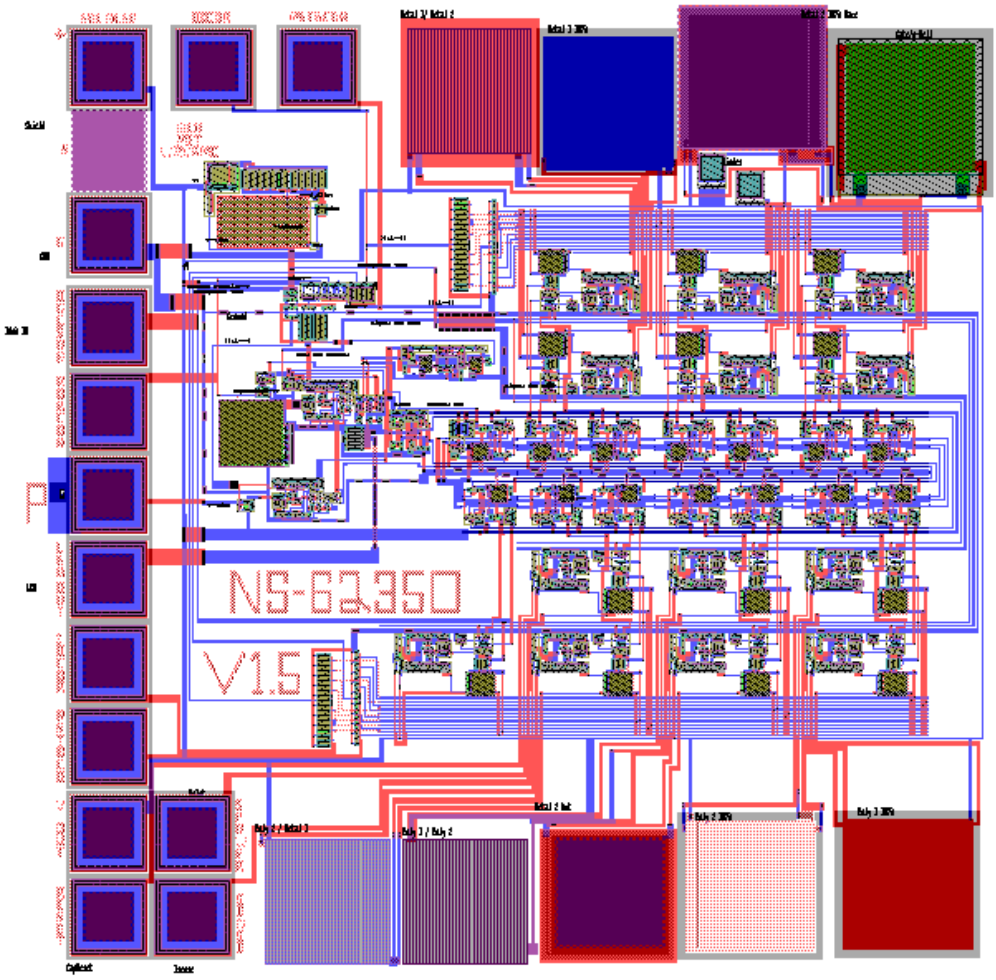


Figure 17: Circuit layout for PassChip CMOS integrated circuit test system.

The chip consists of a Proportional-to-Absolute-Temperature (PTAT) current reference, multiplexed charge integrators, pulse period encoder, and output pulse generator. The test devices, located around the periphery of the chip, were designed to provide sensitive measures of leakage currents between different layers (vertical waffle electrodes) as well as within each layer (lateral IDEs). In addition, a power supply monitor, integrator monitor, and two diode monitors were also included. One external test device can be attached to this chip.

Each device is directly connected to it's own charge integrator which continually integrates until a certain voltage is reached when it resets itself. The output of each integrator is a sawtooth waveform where the negative slope of the output is proportional to the input current, and the constant of proportionality is the integration capacitance. This capacitance can be indirectly measured accurately through the device parameters returned with the chip, but this must be scaled. An appropriate scaling factor can be determined by injecting known currents into the externally connected integrator and observing the changes in slope of the integrator. While the power supply should be quite constant since it is supplied by lithium ion batteries, there will be some variation as time goes on. The circuit is relatively supply independent, but some dependence exists. The voltage dependence of the marker channel is used to monitor the power supply so correction factors can be applied. The circuit also has a temperature dependence due primarily to the PTAT current reference. The reverse biased diodes have a strong temperature dependence that is used to correct for the temperature dependence of the circuit.

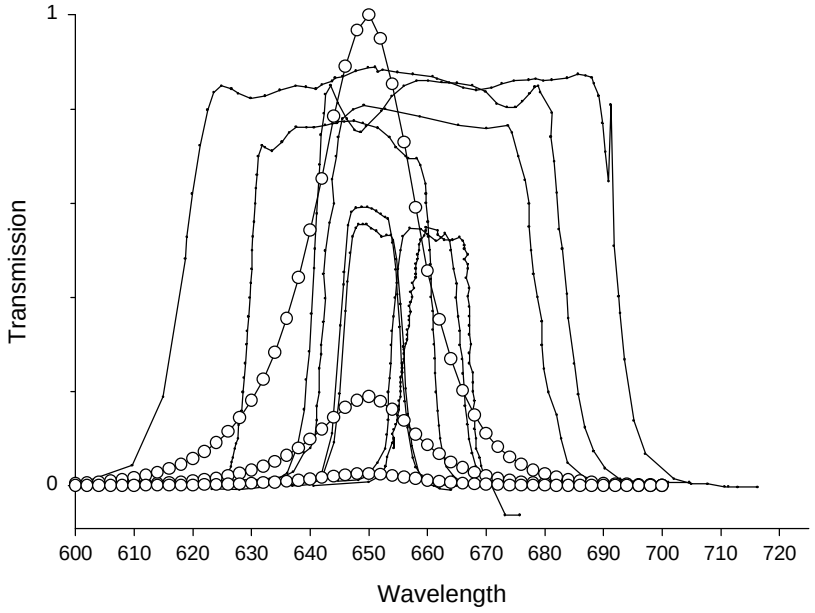


Figure 18: LED emission characterisitcs at 3 intensity levels (Open Circles) and transmission characteristics of a variety of commercially available thin film filters. Narrowband filters shown by arrow were selected to minimize contamination of the data stream by ambient light.

Devices under test typically have two conductors separated by a barrier (insulator or depletion region in the case of the diodes). One conductor provides voltage bias across the barrier as well as power for the integrator reset circuit. The other brings the leakage current to the integrating capacitor as well as providing an electrical path to the integrator reset switch. If either connection fails, the integrator cannot reset and will readout an abnormally low, constant voltage. This architecture eliminates the possibility of obtaining a low leakage reading when in fact the device connection has failed.

The pulse position encoded output from the PassChip directly drives a high efficiency LED for transmission of the data across the skin. A 1cm square photodiode is used to sense the output data pulses. A narrowband filter is used to exclude ambient light while passing the center frequency of the LED. The filter characteristics of available filters are shown in Figure 18. The LED provides a relatively narrowband of output emission. By matching the filter to the characteristic (arrow), the majority of the LED light can be acquired while excluding as much ambient light as possible to avoid saturation of the detector stage. An adaptive threshold detector converts the incoming analog pulses to 5 volt pulses that reset a decoding integrator. The output voltage from the decoding integrator is proportional to the inter-pulse interval, and thus is proportional to the output voltage of the corresponding integrator on the PassChip. A de-multiplexer then reconstructs the output waveforms for each channel, followed by four pole analog filters. The output characteristic of the decoder/demultiplexer with 99% prediction intervals is shown in Figure 19. Note the very low noise associated with this type of signal recovery.

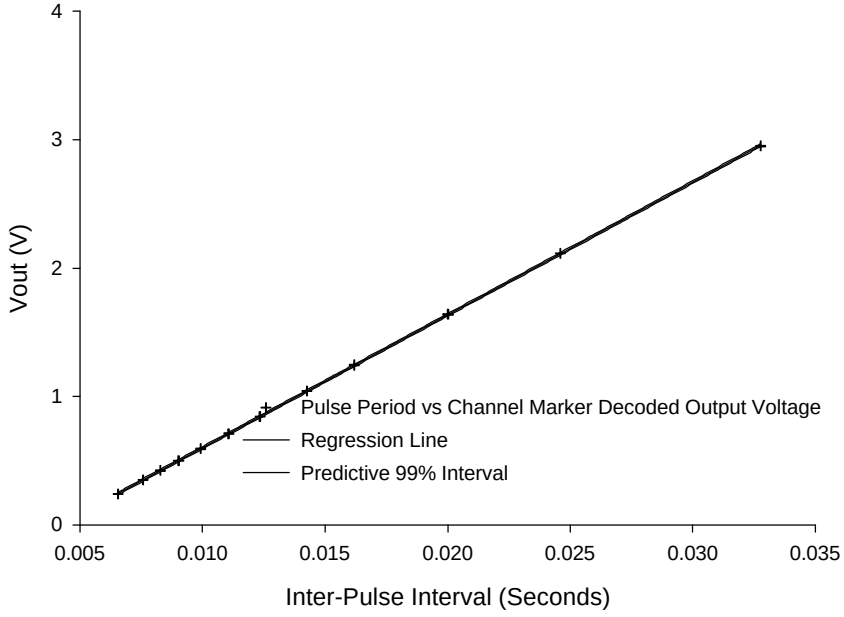


Figure 19: PassChip analog decoder performance.

The passchip is now functional and is being characterized prior to soak testing and implantation. Figure 20 shows the output characteristic of Channel 12, the external input device with about 1pA of injected current. Note the two slopes associated with

the output curve. Previous PassChips exhibited remarkable linearity. This PassChip is different because the voltage range of the output was improved, which now spans the integrator voltage where the depletion region in the N-well is forming under the gate of the capacitor. During the formation of the depletion region, the capacitance is less than that observed in the accumulation region or inversion region because it is the oxide capacitance in series with the depletion capacitance. After the depletion region forms, at low frequencies, the capacitance reverts to the oxide capacitance because the inversion layer can follow the potential changes. To accurately readout these values, it is necessary to wait until the integrator is beyond the inversion formation region. While annoying, this effect does not substantially interfere with operation of these chips. Figure 21 shows data taken with an earlier decoder showing that the output of the channels needs to be below -0.2 volts in order for an accurate measurement to be made. The newer decoder which has different offsets, exhibits the linear response after the output falls below 0.4 volts. It is important to keep in mind that the value of the circuit architecture is that we are making nearly DC measurements of current without having to maintain accurate offsets. It is only the slope of the output characteristics that provide the information. Thus, on-chip amplifier offsets, decoder offsets, filter offsets all have no effect on the accuracy of the data. However, it is important that the slope measurement is accurate, hence the need to wait for the linear region of operation. It should also be noted that subsequent fabrications of similar chips will use a linear capacitor, and may be designed to stay within the 5v process limit rather than the extended 7.3 volts used in this design.

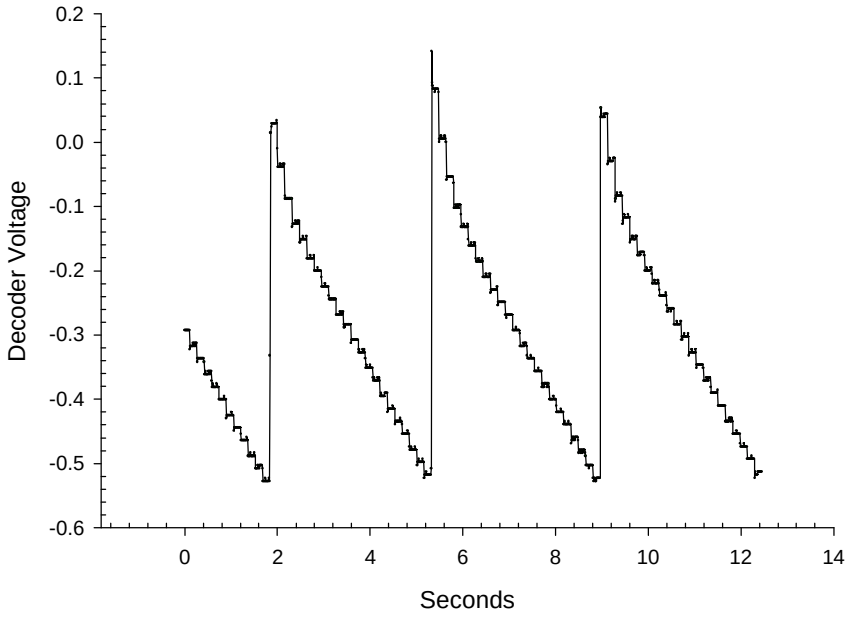


Figure 20: Decoded output voltage from Channel 12 with ~1pA input current. Note the non-linear integrator characteristic. Noise is from defects in an early decoder design.

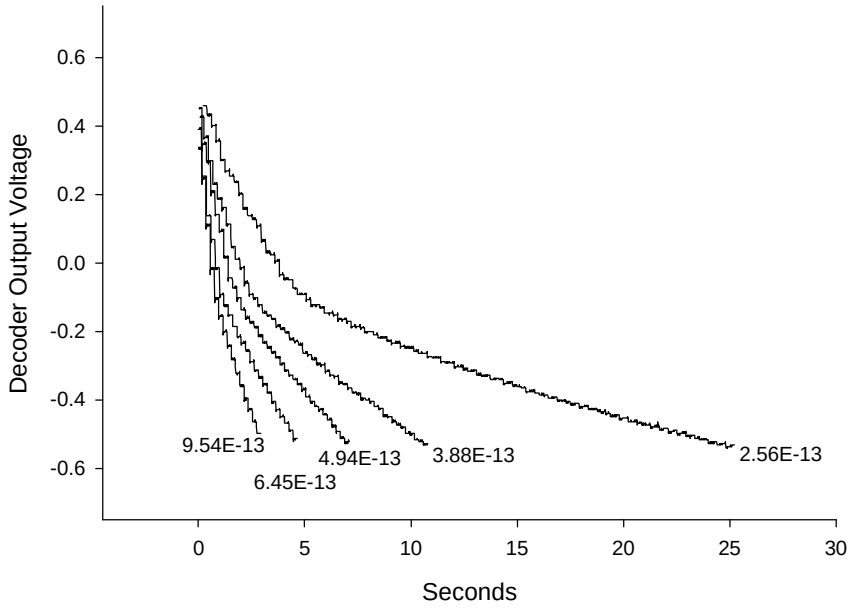


Figure 21: Composite of output waveforms from Channel 12 with various injected currents illustrating non-linearity. Noise is from early decoder design with improper output filtering.

Table 4 shows readings taken from PassChip010699A using approximate calibration numbers. Of particular interest is are the diode leakage current readings and the Poly1-Poly2 waffle patterns. Both of these are large area devices that leak very little. These diodes could be used as input protection devices for high input impedance electrode connections, and also for very sensitive temperature transducers. The Poly1-Poly2 capacitors leak very little as well, and thus could be used to replace the no – linear gate capacitor that was used in this version.

Channel	Description	Reading
Marker	Marker proportional to Vsupply	7.36V
Ch 2	Metal1 IDE with shield	1.20E-15A
Ch 3	Metal1-Metal2 waffle with shield	5.27E-16A
Ch 4	3364 um^2 diode near shield edge	5.10E-15A
Ch 5	3364 um^2 diode	5.01E-14A
Ch 6	Gate waffle on N-well	5.61E-16A
Ch 7	Metal2 IDE bare	2.59E-16A
Ch 8	Poly2 IDE with shield	3.83E-16A
Ch 9	Poly1 IDE with shield	8.10E-17A
Ch 10	Poly1-Poly2 waffle with shield	6.52E-16A
Ch 11	Metal2-outside large pad	9.95E-16A
Ch 12	External injected current	7.59E-13A
Ch 13	Metal1-Poly2 waffle with shield	7.64E-16A
Ch 14	Open circuit integrator	5.58E-16A

Table 4: Preliminary data extracted from PassChip010699A using approximate calibration numbers, room temperature.

Calibration of PassChip010699A was accomplished by injecting various currents into the external device integrator node and computing the resulting slope of the output. Since the transistor thresholds vary only slightly across the chip, and the integration capacitors also are very well matched, only small errors will be incurred by inferring the calibration factor for all channels from this one channel. The channel marker is calibrated independently by varying the supply current. Temperature coefficients for all channels are computed from output data at various chip temperatures holding other variables constant. Figure 22 shows a calibration chart for PassChip 010699A. The lower slope curve is from the inversion region of operation. The higher slope (lower capacitance) curve if from the region where the inversion layer is forming. Multiplying the calibration factor times the slope of the output characteristic yields the leakage current.

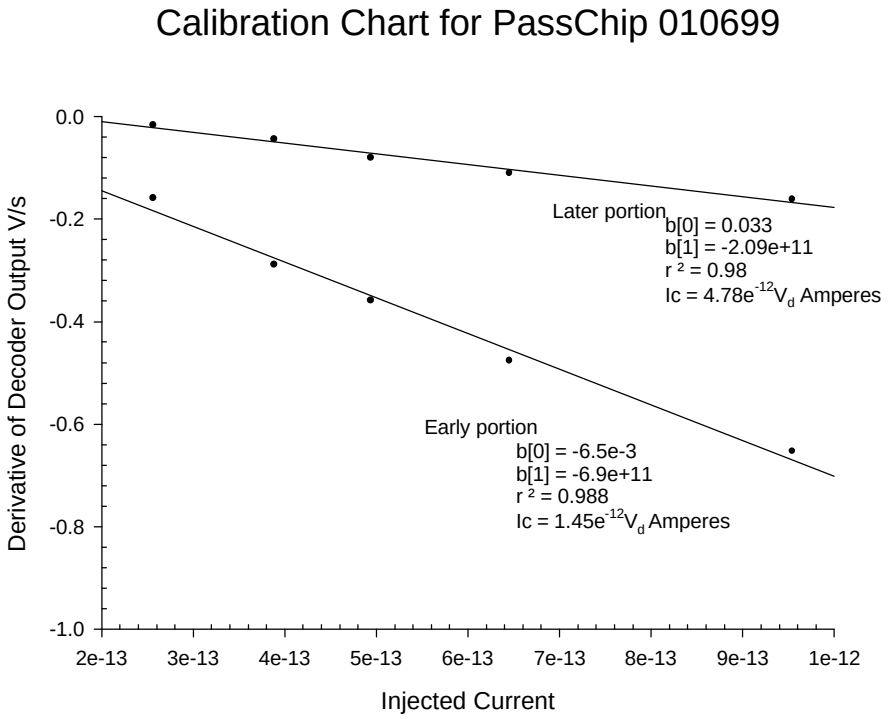


Figure 22: Calibration data for PassChip010699A based on injected current into external device port (Channel 12). Early portion of curve is above output voltage level of about –0.2 volts where inversion layer is forming on the integration capacitor.

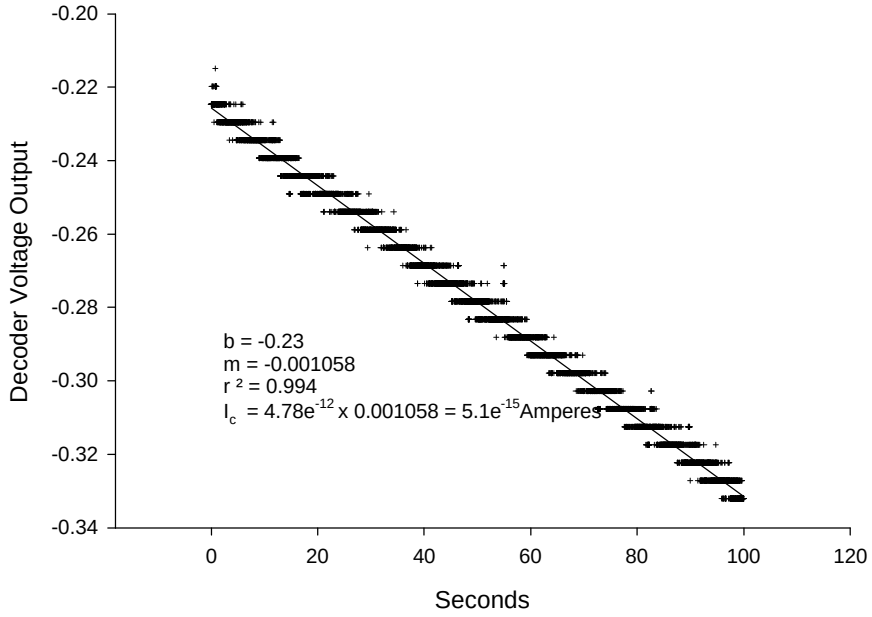


Figure 23: Decoded output of Channel 4 (3364μ^2 diode near shield edge) showing computation of leakage current from decoder voltage output.

Figure 23 shows greater detail of the acquired data set used to compute the output slope of the PassChip for the Channel 4 diode. The overlapping bars are due to quantization errors from the data acquisition system which has a resolution of 5.8mV. By using linear regression to fit a curve to this data, noise variations are averaged out and very accurate computations of the slope can be obtained. Typically, the r^2 value of the correlation is 0.99 or better.

Figure 24 shows a temperature calibration curve for the Channel 4 diode. By computing the slopes of the output for different temperatures, and then computing the regression slope of the temperature vs output slope plot, the temperature coefficient of the data can be obtained. For this example, only 3 temperatures were measured, and the data set was not as extensive as it could be for accurate measurements, but still the temperature relationship is apparent, and illustrates how sensitive these diode leakage currents are to temperature variations.

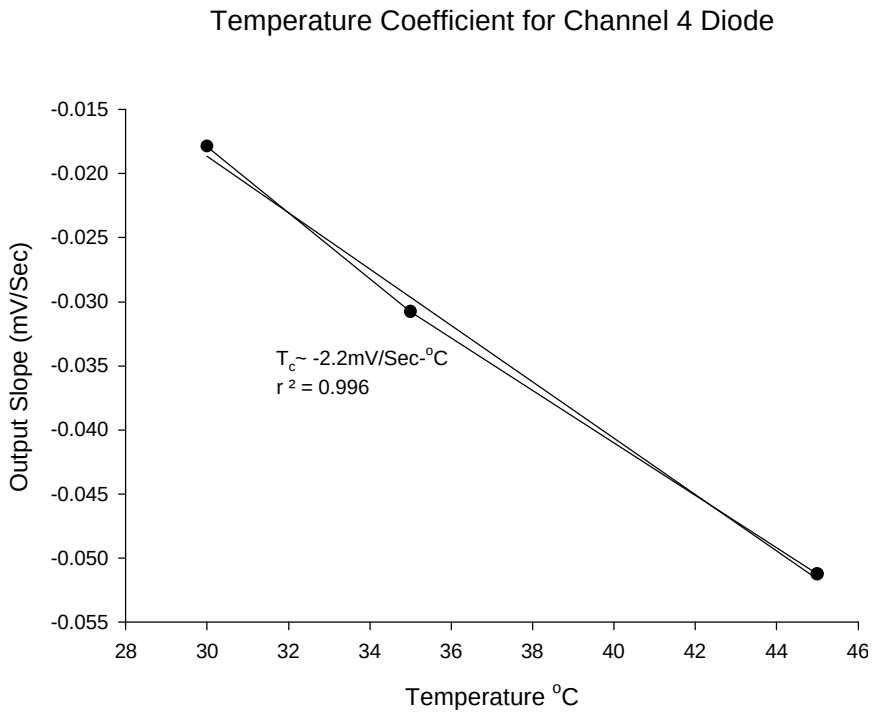


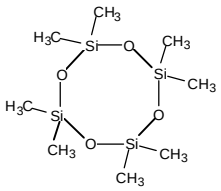
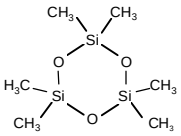
Figure 24: Temperature relationship for Channel 4 diode on PassChip010699A.

Additional analyses and documentation are needed to fully characterize this chip. Once these are accomplished, and the system is thoroughly proven, devices will be assembled and placed under saline soak. Successful saline soak for 4 weeks will be followed by implantation in rabbits complete with telemetry and battery supply.

Accomplishments: HFCVD of silicone thin films.

We have demonstrated for the first time a pyrolytic process for the deposition of silicone thin films from the low-pressure thermolysis of octamethylcyclotetrasiloxane, $[(CH_3)_2SiO]_4$, also known as D_4 from the commonly used nomenclature of D for $–(CH_3)_2SiO–$. D_4 is a monomer which is commonly used in the base catalyzed, liquid phase ring-opening polymerization for PDMS. In addition, D_4 melts at 17 °C and hence is a liquid at standard conditions with a reasonable vapor pressure. HFCVD was also achieved from a second monomer, D_3, which is a solid at ambient conditions. In the HFCVD method the cyclic monomers are decomposed over a hot-filament. High deposition rates (up to 2.5 µm/min) could be achieved.

Table 1: Chemical structure and properties for silicone CVD feed gases.

Structure	Name	Boiling Point	Vapor Pressure
	D_4	175°C	1 torr @ 23°C
	D_3	134°C	70 torr @ 70°C

In our experiments, approximately 2 sccm of D_4 or D_3 was vaporized through the reactor chamber by mildly heating a Pyrex container attached to a valve on the chamber. Pressure was maintained at 0.6 torr by adjusting a throttle valve on the reactor outlet. A 1 mm diameter tantalum wire was resistively heated to between 260 and 530 °C for these experiments. The substrate was a 2" Si wafer sitting 11 mm away on a water cooled stage; the temperature as measured by a thermocouple on the backside of the wafer was 20 ± 3 °C. The growth rate in the center of the substrate varied from $2.5x10^4$ to 5 Å/min depending on the filament temperature. By comparison, the maximum deposition rates reported for the plasma polymerization of hexamethyl-disiloxane varied from 0.5 µg cm^{-2} s^{-1} for capacitively coupled discharges to 2.6 µg cm^{-2} s^{-1} for microwave discharges, which translates to linear growth rates of about $3x10^3$ and $1.6x10^4$ Å/min, respectively (Fig. 1)

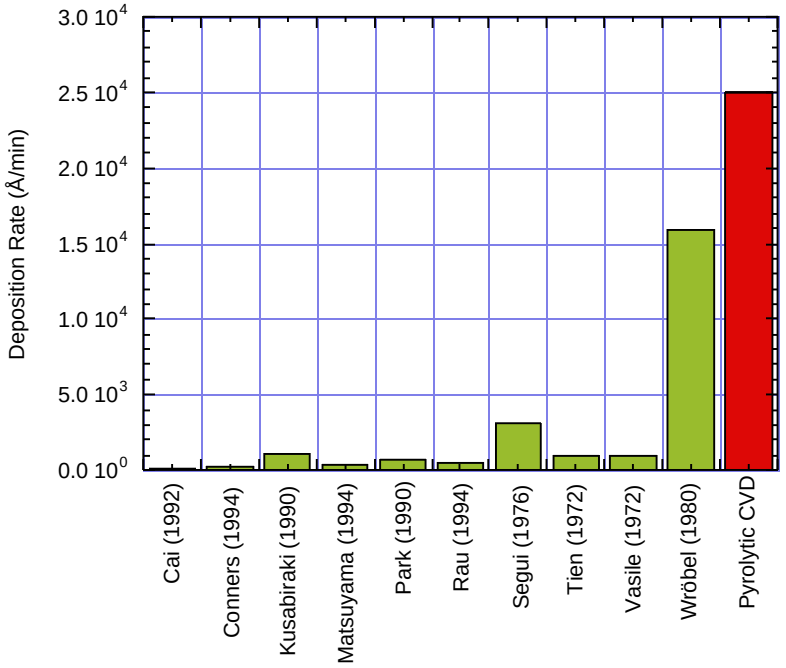


Figure 1. Deposition rates for standard PECVD processes versus that for the new HF (pyrolytic) CVD.

Fourier transform infrared spectroscopy (FTIR) verified that the deposited films had the same functional groups as a PDMS standard, though with a measurably lower methyl concentration (Fig. 2). In order to permit semi-quantitative analysis, the FTIR spectra are shown in normalized absorbance units. The main feature to note in this case is the marked difference in relative intensity between the CVD film and the standard at 2964 cm^{-1}, 1410 cm^{-1}, and 702 cm^{-1}. The peaks at 2964 cm^{-1} and 2906 cm^{-1} are due to the asymmetric and symmetric C-H methyl stretches, respectively, while the peak at 1410 cm^{-1} is the result of the C-H methyl bending modes. This implies that the CVD film is deficient in methyl substituents as compared to the PDMS standard. We can also rule out the loss of sp^3-CH_3 absorption intensity due to any C-C crosslinking since such a rearrangement would result in the appearance of new peaks in the C-H stretch region at a lower wavenumber corresponding to sp^3-CH_2. The peak at 702 cm^{-1} is in a region which is typically assigned to Si-C stretches.

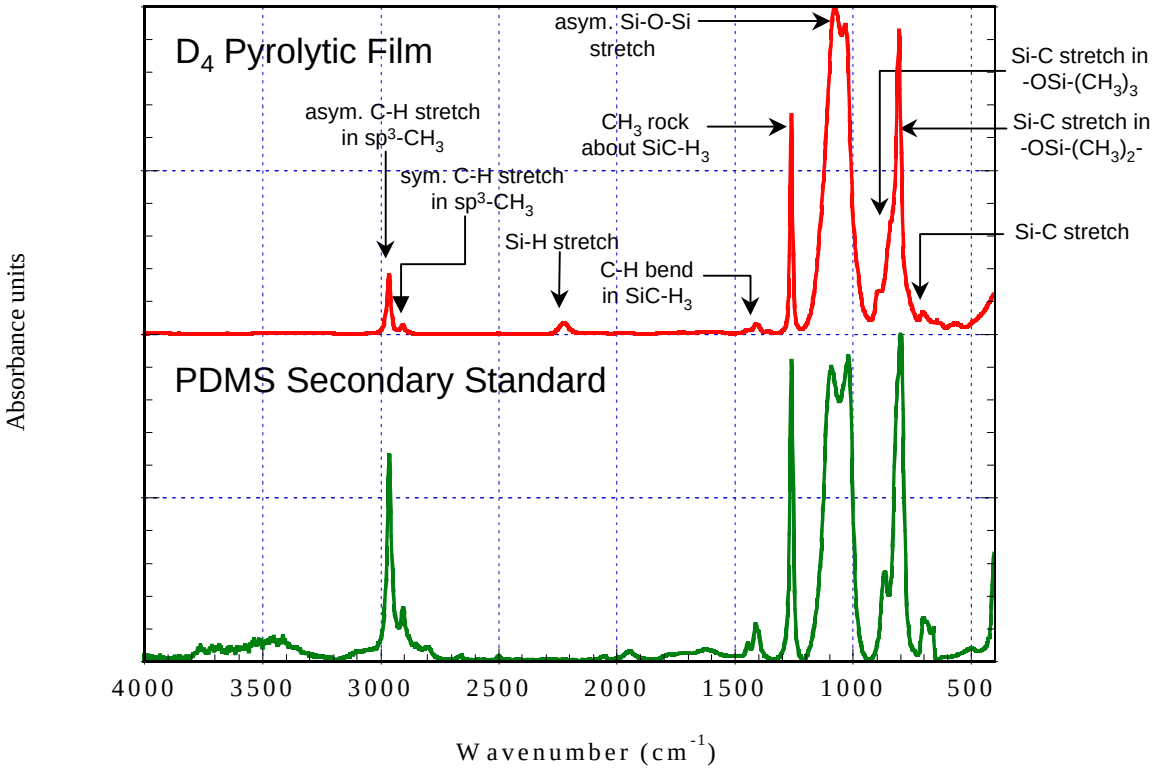


Fig. 2: Comparison of FTIR spectra of a 6.9 µm thick HF (pyrolytic) CVD thin film with a poly(dimethylsiloxane) (PDMS) standard

An X-ray photoelectron spectroscopy (XPS) survey scans showed that a typical film had an elemental composition of C:Si:O / 1.5:1:1, confirming the loss of methyl groups as shown by FTIR spectroscopy. Higher resolutions Si2p XPS spectra show that the Si-O backbone is left intact by the deposition process. The loss of methyl groups may lead to crosslinking in the films. To examine this hypothesis further, solubility tests on as deposited thin films were conducted in benzene, toluene, and a mixture of xylene isomers. In all cases, the weight loss was minimal, being less than 10% and limited by the resolution and accuracy of the balance.

Further chemical analysis was carried out by solid-state ^{29}Si nuclear magnetic resonance (NMR) (Fig. 3). The NMR confirms crosslinking groups (new peak) in the HFCVD film do not have the same chemical structure as conventional PECVD films. Also, the NMR reveals that the siloxane backbone is the predominate bonding environment in the HFCVD film.

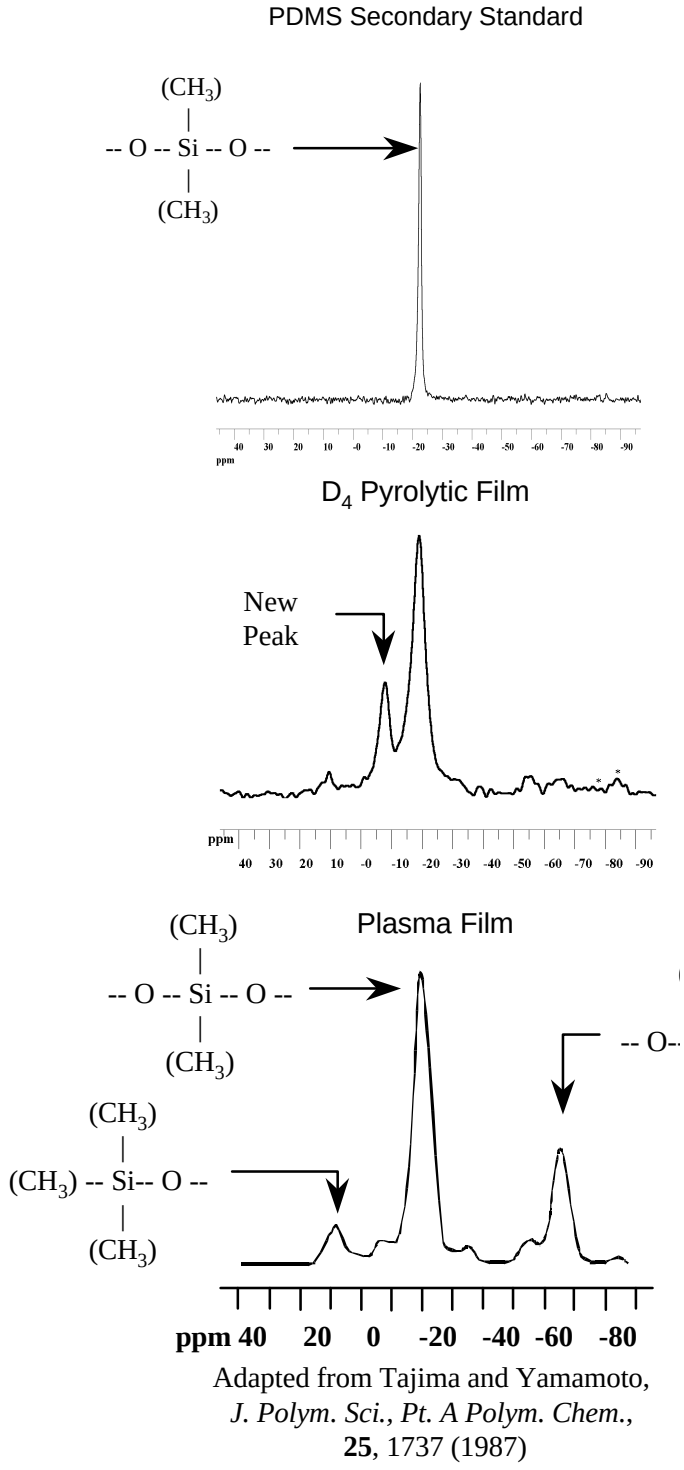


Fig. 3. Solid-state ^{29}Si NMR showing predominance of the siloxane backbone in the pyrolytic CVD film. Also note the contrast in crosslinking structure between the pyrolytic and plasma films.

In order to better understand the kinetics of this process, the growth rate was measured at several filament temperatures and the results plotted in Arrhenius form. For films under approximately a micron in thickness, the deposition rate was measured by ellipsometry. Thicker films were measured by scratching the film and using a stylus profilometer. Figure 4 is a graph of the natural log of the growth rate versus the reciprocal of the filament temperature. A linear fit to the data is shown and yields an activation energy of 36.5 ± 4 kcal/mol.

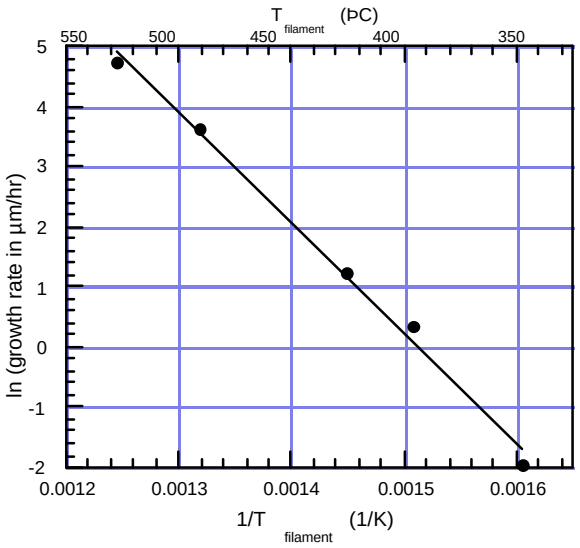


Figure 4. Arrhenius plot for pyrolytic CVD at 0.6 torr

In contrast to PECVD, HFCVD does not involve any ion bombardment or UV irradiation thus eliminating the possibility of related atomic rearrangements and defects. The ability to grow fluorocarbon and silicone thin films by pyrolytic CVD reveals that ion bombardment, which is often cited in discussions of PECVD mechanisms as being essential to the creation of active sites for film growth, is in fact not necessary for the deposition of these materials. In addition, very high silicone growth rates have been achieved by pyrolytic CVD.

Fig. 5a shows that the HFCVD wire coatings from D_3 exhibit good flexibility, with the films remaining intact after the deformation of the wires into loops. Cross-sectional images (Fig. 5b) show no chipping of the coating or gaps between the wire substrates and the coating.

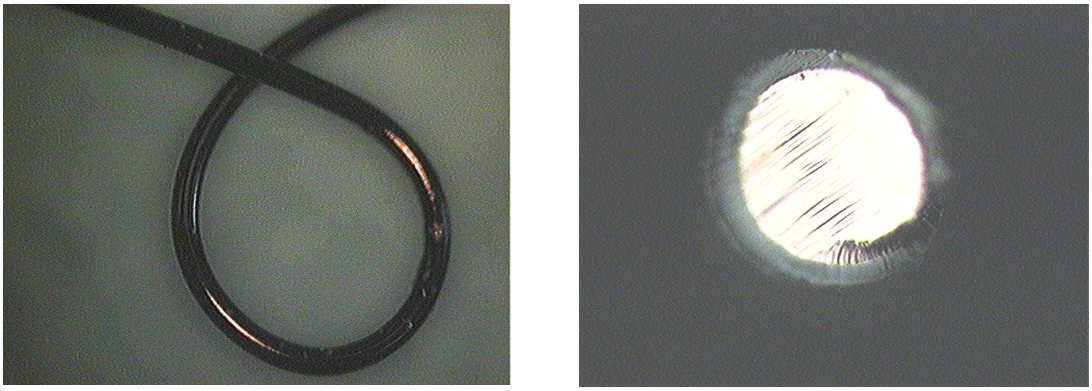


Fig. 5. Optical micrographs of coatings on 3 mil Cu wires produced by HFCVD from D_3. Fig. 5a (left) shows the coating to be flexible with no cracking when a loop is formed in the wire. Fig. 5b (right) shows a cross-sectional view after the coated wire was cut by a razor. Adhesion is good as no gap spaces are formed between the wire and the coating, which is approximately 10 mm thick.

Accomplishments: Pulsed-PECVD Organosilicon Films

We have used pulsed-plasma enhanced chemical vapor deposition (PPECVD) to deposit films from the organosilicon precursors D_3 and D_4. A parallel-plate plasma deposition system was employed, with a powered upper electrode and a grounded lower electrode and chamber. The precursor was vaporized in a heated vessel and flow controlled using a needle valve to maintain a flow rate of about 8 sccm. Argon was used as a diluent and the flow rate was maintained at approximately 40 sccm. Substrate temperature was maintained at ambient by cooling water. Peak power during on-time excitation was 280 W.

Table AA: Films deposited using precursor D_4, octamethylcyclotetrasiloxane

Sample Name	Deposition Conditions	Est. Max. Thickness
LL-1 (05/16/98A)	60 min @ CW	Sample no good
LL-2 (05/18/98B)	50 min @ CW	5.5 μm
LL-3 (05/19/98A)	60 min @ 10/100	1.3 μm
LL-4 (05/20/98A)	50 min @ 100/400	2.6 μm

Table BB: Films deposited using precursor D_3, hexamethylcyclotrisiloxane

Sample Name	Deposition Conditions	Est. Max. Thickness
LL-5 (05/21/98C)	60 min @ CW	3.8 μm
LL-6 (05/22/98A)	60 min @ 100/400	2.5 μm
LL-7 (05/24/98A)	38 min @ 10/100	0.9 μm
LL-8 (08/07/98A)	50 min @ 100/600	1.0 μm
LL-9 (08/07/98B)	90 min @ 10/250	0.5 μm
LL-10 (08/07/98C)	50 min @ 10/60	0.6 μm
LL-11 (08/10/98A)	52 min @ 100/400	1.5 μm
LL-12 (08/11/98A)	60 min @ 100/400	2.4 μm
LL-13 (08/11/98B)	60 min @ 10/100	0.7 μm
LL-14 (08/11/98C)	50 min @ CW	1.6 μm
LL-15 (08/13/98A)	60 min @ 100/200	4.4 μm
LL-16 (08/14/98A)	50 min @ 10/60	1.1 μm

Initially, films were deposited from both D_3 and D_4 onto clean ½" silicon substrates at three different pulse duty cycles: continuous wave excitation (CW), 10 ms on/ 100 ms off (10/100), and 100 ms on/400 ms off (100/400). These films underwent preliminary saline soak testing, and no significant differences were noted between the resistivities of the films from either precursor. It was decided to focus our efforts on D_3 as a precursor as it was simpler to handle as a solid at room temperature and showed more consistent deposition rates. Further films were deposited at pulse duty cycles varying from CW excitation to 10/250. In addition, films were deposited at 10/60 and 100/600 to try to observe the effect of on-time and off-time on film composition. Table AA and Table BB show the deposition conditions and estimated maximum thickness of the films produced from D_4 and D_3 for soak testing at Lincoln Lab.

We anticipate that as the pulse duty cycle decreases, the degree of crosslinking in the plasma films should decrease, leading to greater film flexibility. Films were thus deposited under varying conditions onto 3-mil copper wires (0.003" diameter), which were strung across an aluminum ring placed on the lower electrode. Following deposition, an optical microscope was used to estimate the film thickness and to observe the behavior of the films when the wire was twisted around a mandrel 750 μm in diameter. Cracking and flaking of the films was taken to indicate poor flexibility.

Figure 6 shows the results of wire loop testing for films deposited from D_3 under conditions of continuous wave excitation and a pulsed duty cycle of 14 %. The CW film exhibited considerable flaking under tension, while the films of lower duty cycle showed improved flexibility. In particular, cracking and flaking was reduced as the on-time and off-time was increased, as illustrated by the good flexibility of the 100/600 film.

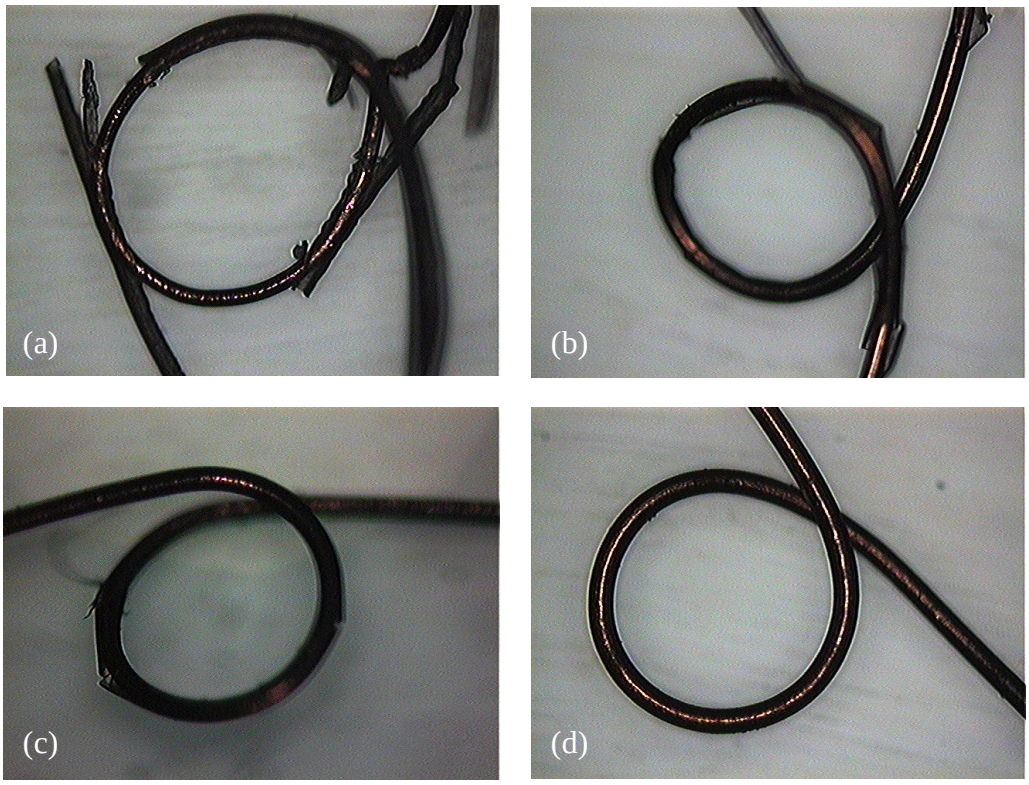


Figure 6: 750 ㎜ loops of 3-mil copper wire coated with D_3 pulsed-plasma film at (a) CW, (b) 10/60, (c) 50/300, and (d) 100/600.
Film thicknesses are (a) 19 ㎜, (b) 9 ㎜, (c) 12 ㎜ and (d) 13 ㎜.

One of the ultimate objectives of this work is to demonstrate complete encapsulation of an implantable IC assembly with a biocompatible insulating layer. However, implantable devices such as UM probes are relatively expensive and time-consuming to prepare for coating. To test our ability to coat assemblies consisting of both planar circuitry and wires quickly and cheaply, we produced dummy assemblies similar to that shown in Figure 7. The assembly was made from a cleaved 2" wafer and five 3-mil copper wires which were glued to the wafer. The thickness of the coating on the silicon wafer could then be measured using profilometry or ellipsometry, and the thickness of the film on the wires using an optical microscope. Coated wire was cut off the assembly and cross-sectional views obtained under 20x magnification at various points along the length of the wire. This allowed us to observe the thickness profile along the wire from the highest point – about 2 cm above the wafer – to the junction with the wafer.

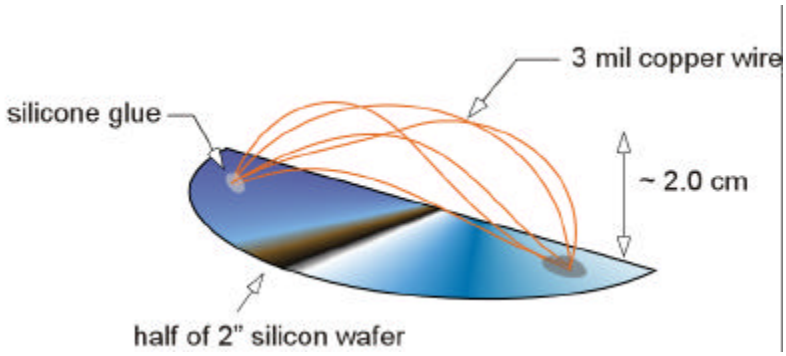


Figure 7: Triple-track and UM dummy test assembly

It was observed that there was a significant disparity between deposition rates on the wires and on the wafer segment. Specifically, it was noted that the maximum thickness of film on the wires was almost an order of magnitude greater than that on the wafer below it. Whereas the coatings on the wires were of the order of 10 μm at the thickest point, the maximum film thickness on the wafer was about 1 μm. The thickness of the coating on each wire decreased from a maximum at the middle and highest point to the approximate thickness of the film on the wafer close to the junction bond. Furthermore, the film on the wafer segment showed thickness non-uniformity corresponding to the pattern of the wires suspended above it. It appears as if the wires exert some kind of influence on film growth on the wafer. Despite the wires being quite close to each other at points – 2 to 3 mm for the most part – the thickness of coatings at each point along the wires was conformal and showed no evidence of similar non-uniformity.

To determine if the observed disparity in deposition rates and non-uniformity was an indication of a mass-transfer limitation during film growth from the vapor phase, the flow rate of the diluent gas argon was increased. It was found that growth rates could be significantly improved by doing this, but the difference in deposition rates between wire and wafer remained about the same. Argon flows greater than 120 sccm were found to produce no further increase in growth rates, but the disparity remained an order of magnitude. Helium was also tested as a diluent gas and produced similar results. Further coatings were performed at a higher argon flow rate to improve deposition rates and reduce the time required to produce films. Since higher flow rates reduce the residence time of reactive gases in the chamber, the plasma pulsing conditions were adjusted appropriately. In particular, depositions performed at 100/600 at an argon flow rate of 40 sccm were performed at 50/300 at an argon flow rate of 80 sccm. Due to the higher argon flow, the deposition rate improved from 1,800 Å/min to 3,500 Å/min.

An UM probe was coated to observe the conformity of film around small features. Figure 8 shows an ESEM micrograph of the tines of the coated probe. Film thickness is around 20 μm and the film is observed to have coated all visible features. The probe itself was many months old and particles of dirt appear to have been incorporated into

the growing film. Cleanliness of the deposition environment is an important imperative that has been addressed in the design of the new CVD reactor.

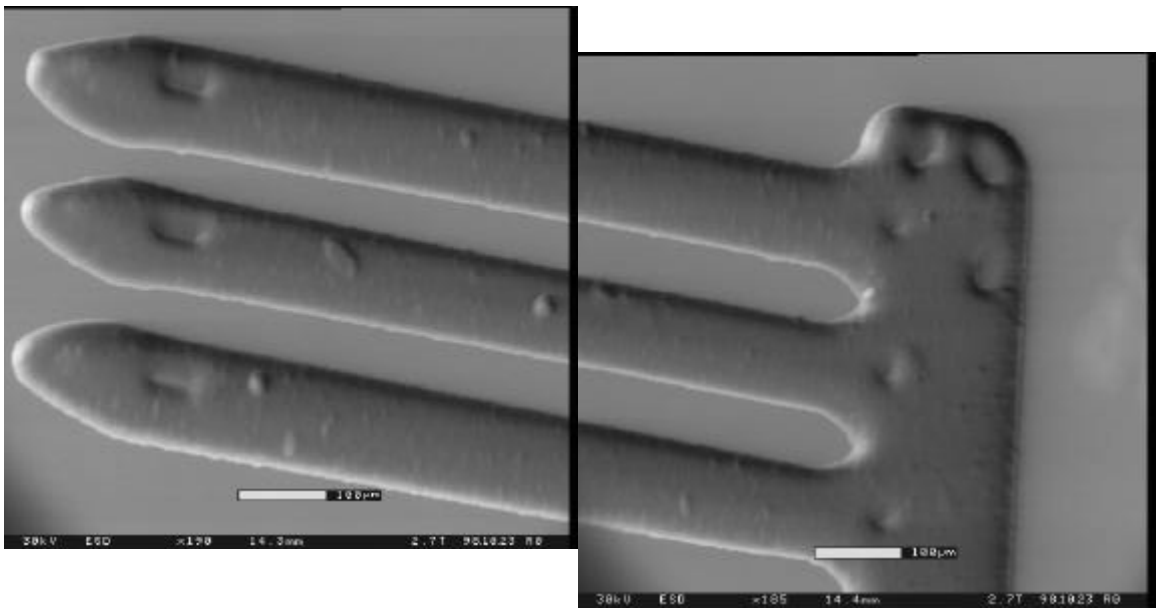


Figure 8: Tines of UM probe coated with pulsed-plasma film from D_3 for 50 min at 50/300

Some fully-assembled test devices have been coated successfully for soak testing by Dave Edell. These were devices with circuitry mounted on a glass slide and wires running from bond pads to a common connector. Two configurations were used for the triple-track assemblies: one in which the triple-track was mounted directly on the slide and another in which two triple-tracks were mounted side-by-side elevated about 1 cm above the slide. This was done to determine how elevation in the plasma affected the deposition rate. Bonded UM probes were also similarly prepared and coated. Figure 9 is an ESEM micrograph showing the bond pads from one of the UM probes. The coating is too thin to be obvious, and some work needs to be done to try to obtain a thicker coat around the pads, which are areas requiring good encapsulation.

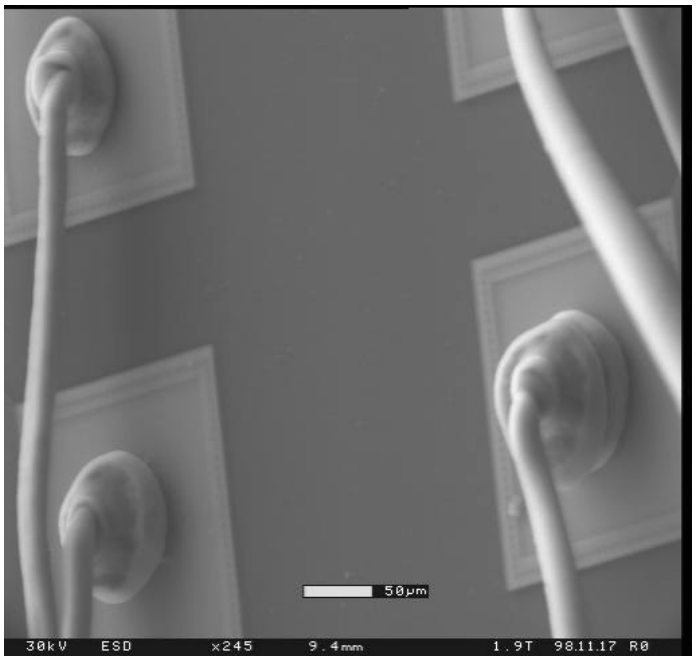


Figure 9: Bond pads of UM probe assembly coated with pulsed-plasma film from D_3 for 50 min at 50/300

Accomplishments: Design for uniform HFCVD

Our design, shown in Fig. 10, has allowed HFCVD films to be deposited uniformity onto silicon wafers. For fluorocarbon HFCVD, the variation in film thickness is <10% over a 4" diameter substrate. Water backside cooling of the substrate allows it to remain at room temperature. Similar fixtures for the hot filaments allow for HFCVD coating of 3D substrates.

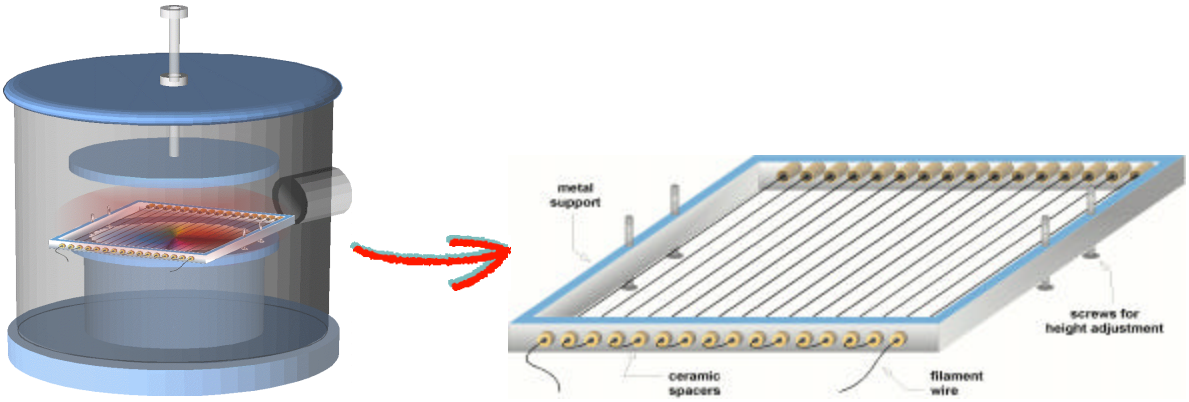


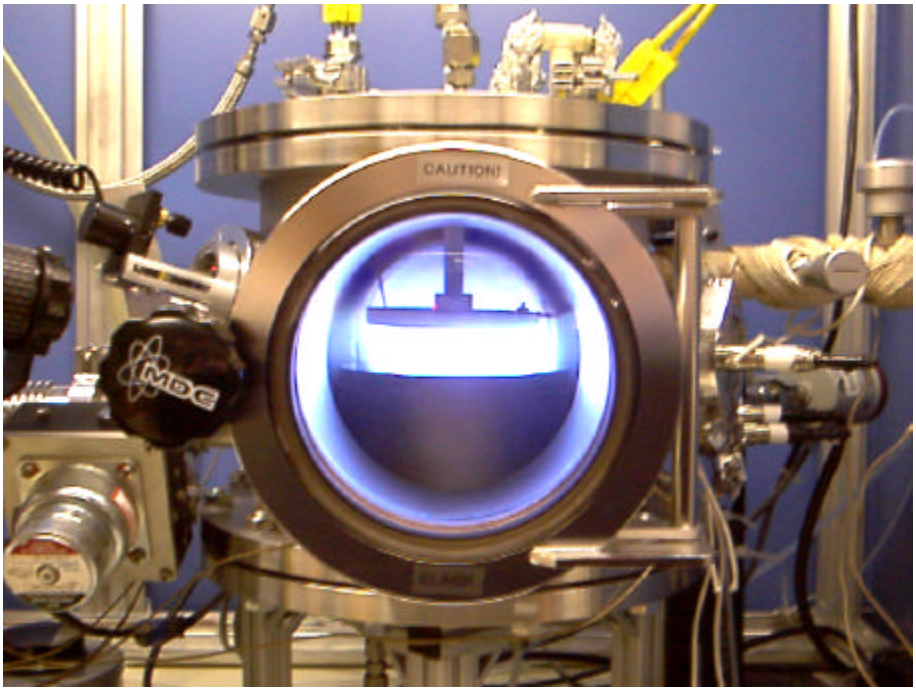
Figure 10. Schematic diagram of the filament setup for pyrolytic CVD. Filament wire is resistively heated to the required precursor gas decomposition temperatures

Accomplishments: Construction of new CVD reactor

A new CVD reactor system has been fabricated. Figure 11 shows the design of the vacuum chamber in the new setup. It is a parallel-plate reactor along the lines of the system previously used for depositing fluorocarbon and organosilicon films. However, it incorporates some major improvements over the old system. In particular, the addition of a large (8") front access door with viewport makes for easier sample loading and unloading. In the previous system, the entire lid of the reactor had to be removed to allow sample placement. This access door also leads to a cleaner working and deposition environment: during sample transfer, a positive nitrogen pressure can be employed in the chamber to exclude dirt and dust particles. The chamber itself is larger than in the previous system and thus has the ability to coat more substrates simultaneously, reducing turnover time.

The new chamber was also designed with many more ports than the previous system specifically to enable *in situ* CVD diagnostics. Such diagnostics will greatly enhance our understanding of the CVD reaction environment. Two viewports angled at 15° to the horizontal were added to accommodate future addition of a laser interferometry system to measure the real-time deposition rate. The 8" port at the back of the reactor could be used for a mass spectrometer. It has a copper gasket seal that is suitable for the installation of a turbopump, and the port is sufficiently large to allow the possibility of vertical and horizontal resolution of the species profile in the plasma.

Another port, having a sapphire window, will be used with our new optical emission spectrometer (OES).



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October 1996 - September 1999

1. S. J. Limb, C. E. Labelle, K.K. Gleason, E.F. Gleason and D.J. Edell, *"Growth of Fluorocarbon Polymer Thin Films with High CF_2 Fraction and Low Dangling Bond Concentration by Thermal Chemical Vapor Deposition"*, Appl. Phys. Lett. **68**, 2810 (1996).
2. S.J. Limb, K.K. Gleason, D.J. Edell and E.F. Gleason, *"Flexible Fluorocarbon Wire Coatings by Pulsed Plasma Chemical Vapor Deposition"*, J. Vacuum Sci. Technol. A **15**, 1814(1997).
3. C.B. Labelle, S.J. Limb and K.K. Gleason, *"Electron Spin Resonance of Pulsed Plasma Enhanced Chemical Vapor Deposited Fluorocarbon Films"*, J. Appl. Phys **82**, 1784 (1997).
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7. M.C. Kwan and K.K. Gleason, *"Pyrolytic Chemical Vapor Deposition of Poly(dimethylsiloxane) Thin Films"*, Advanced Materials: Chemical Vapor Deposition **6**, 299 (1997).

8. M.C. Kwan and H.G. Pryce-Lewis, *"Pyrolytic Chemical Vapor Deposition of Poly(organosiloxane) Thin Films"*, Silicones in Coatings Conference Proceedings, Orlando, Feb. 1998
9. S.J. Limb, D.J. Edell, E.F. Gleason and K.K. Gleason, "*Comparison of Pulsed Plasma Enhanced Chemical Vapor Deposition and Pyrolytic Chemical Vapor Deposition from Hexafluoropropylene Oxide"*, Plasmas and Polymers 4(1), 21 (1999)

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October 1996- September 1999

1. *"Pulsed-Plasma Polymer Deposition"*, Defense Sciences Research Council (DSRC), La Jolla, July 1996.
2. "*Novel CVD of "Teflon"-Like Insulating Biomaterials"*, American Vacuum Society 43rd Annual Meeting, Philadelphia, October 1996.
3. "*CVD of Teflon-like Thin Films"*, Lam Research, Fremont, CA, October 1996.
4. "*Pulsed Plasma Enhanced and Pyrolytic CVD of Low Dielectric Constant Fluorocarbon Films"* Intel, Santa Clara, February 1997.
5. "*Novel CVD of Polymeric Thin Films"* Perkin-Elmer, Applied Biosystems, Foster City, CA, February 1997.
6. "*Pulsed Plasma Enhanced and Pyrolytic CVD of 'Teflon-like' Thin Films"*, North Carolina State University, Department of Chemical Engineering, February, 1997.
7. "*Pulsed Plasma Enhanced and Pyrolytic CVD of 'Teflon-like" Thin Films'*, Becton Dickinson Research Center, Research Triangle Park, NC, February, 1997.
8. "*Pulsed Plasma Enhanced and Pyrolytic CVD of 'Teflon-like' Thin Films"*, Dupont, March 1997.
9. "*NMR of Pulsed Plasma and Pyrolytic CVD Fluorocarbon Films"*, 1997 Federation of Analytical Chemistry and Spectroscopy Societies, Providence, RI, October 1997.
10. "*Pulsed Plasma and Pyrolytic CVD of Low Dielectric Constant Fluorocarbon Films"*, Tokyo Electron Limited (TEL) Tokyo, April 1997.
11. "*Pulsed Plasma Enhanced Chemical Vapor Deposition form $C_2H_2F_4$, CH_2F_2, and $CHC1F_2$"*, Materials Research Society Spring Meeting, San Francisco, April 1998.
12. "*Pulsed Plasma and Pyrolytic CVD of Fluorocarbon and Organosilicone Films"*, Naval Research Laboratory, November, 1998.
13. "*Low Dielectric Constant Fluorocarbon Films"*, Materials Research Society Fall Meeting, Boston, December 1998.
14. "*Controlling and Characterizing the Molecular Architecture of Fluorocarbon Thin Films by Chemical Vapor Deposition (CVD)"*, Stanford University, Dept. of Chemical Engineering, Stanford, January 1999.
15. "*Controlling and Characterizing the Molecular Architecture of Fluorocarbon Thin Films by Chemical Vapor Deposition (CVD)"*, Colorado State University, Dept. of Chemical Engineering, January 1999.
16. "*Controlling and Characterizing the Molecular Architecture of Fluorocarbon Thin Films by Chemical Vapor Deposition (CVD)"*, Colorado School of Mines, Dept. of Chemical Engineering, Golden, CO, January 1999.
17. *"Fast MAS and Multidimensional NMR of Fluorocarbon Chemically Vapor Deposited Thin Films",* International Symposium on the NMR Spectroscopy of Polymers, Breckenridge, CO (sponsored by the Polymer Division of the ACS), January 1999.

18. *"Pulsed Plasma Enhanced and Pyrolytic Chemical Vapor Deposition of Fluorocarbon Films"*, Fluorine in Coatings III Conference, Orlando, FL, January 1999.
19. *"Controlling and Characterizing the Molecular Architecture of Pulsed Plasma and Pyrolytic Chemical Vapor Deposition (CVD) Fluorocarbons and Organosilicones",* First Alpine International Symposium on Plasma Processing of Polymers (Riccardo d'Agostino, chair), Campitello di Fassa, Italy, January – February 1999.
20. *"The History and Future of Fluorocarbon CVD Dielectric Thin Films",* Dielectrics for ULSI Multilevel Interconnection Conference (DUMIC), San Jose, CA, February 1999. **Keynote Address**
21. *"CVD of Fluorocarbon Low-k Dielectric Films"*, Gordon Research Conference on Electronic Materials, New England College, Henniker, NH, July 1999.
22. *"Low Dielectric Constant CVD Fluorocarbon Films"*, National ACS Meeting, PMSE-Symposium on Micro- and Nano-Patterning Science and Technology, New Orleans, August 1999.